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RSi4000 VALIDATION TESTS

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By

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By

J. Ryan, S. Motty, M. Johnson

Sigma Engineering Limited

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Un sommaire français se trouve avant la table des matières.

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16. Abstract

The RSi4000 radar interface card was developed in 2001 to provide improved data quality and detection performance when used in conjunction with the SeaScan Radar processor (formally referred to as the Modular Radar Interface). In order to characterize the RSi4000's performance, a quantitative validation program was undertaken in 2002. This validation included laboratory tests on the RSi4000 radar interface and field trials on iceberg targets. The field trials were conducted in June and July 2002 at Twillingate, Newfoundland, using a mobile radar unit with high-speed radar antenna.

In general, it was found that the new radar interface provided excellent signal-to-noise ratio performance in laboratory tests and demonstrated that, with the application of pulse-to-pulse processing, it is possible to get in excess of 11 bits of amplitude resolution from the system.

Field trials on numerous iceberg targets demonstrated that, with the application of scan-to-scan processing techniques, the system is capable of detecting growler- and bergy bit-sized targets in heavy seas.

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16. Résumé

La carte d'interface radar RSi4000 a été mise au point en 2001 pour améliorer la qualité des données et la performance de détection, lorsque jumelée au processeur radar SeaScan (autrefois désigné *interface modulaire radar*). Pour caractériser la performance de l'interface RSi4000, un programme de validation quantitative a eu lieu en 2002. Ce programme comprenait des essais en laboratoire de l'interface radar RSi4000 ainsi que des essais de détection d'icebergs réels. Ces essais sur le terrain ont eu lieu en juin et juillet 2002 à Twillingate, Terre-Neuve, à l'aide d'un radar mobile couplé à une antenne radar haute vitesse.

Les essais en laboratoire de la nouvelle interface radar ont permis d'enregistrer un excellent rapport signal/bruit. Par ailleurs, grâce au traitement d'une impulsion à l'autre, il a été possible d'obtenir une résolution d'amplitude d'au moins 11 bits.

Les essais sur le terrain, qui avaient pour cibles des icebergs, ont révélé que, grâce aux techniques de traitement d'un balayage à l'autre, le système pouvait détecter des bergy bits et des bourguignons dans des conditions de grosse mer.

17. Mots clés	18. Diffusion
Détection d'icebergs, détection de petites cibles dans un clutter intense, traitement de signaux radar, interface radar, conversion de balayage radar, filtre d'impulsion, antenne radar haute vitesse	Le Centre de développement des transports dispose d'un nombre limité d'exemplaires.

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EXECUTIVE SUMMARY

The RSi4000 radar interface card was developed in 2001 to provide improved data quality and detection performance when used in conjunction with the SeaScan Radar processor (formally referred to as the Modular Radar Interface). In order to characterize the RSi4000 performance, a quantitative validation program was undertaken in 2002. This validation included laboratory tests on the RSi4000 radar interface and field trials conducted in June and July 2002 in Twillingate, Newfoundland.

In preparation for the field trials, repairs were made to the Raytheon Pathfinder MK2 radar to correct problems that had developed during the *Kometik* trials of 2000. The radar equipment was then mounted on top of a modified cube van that was outfitted to provide a permanent, mobile platform for these and future data collection trials.

During the intermediate phase of the project, Sigma undertook the development of a new composite video decoder (CVD) card. The CVD is an integral part of the system using the Raytheon MK2 high-speed scanner. It extracts angle and status information from the radar video and converts it to a format compatible with the RSi4000RT. While the CVD requires only power from the host computer, the previous version required an ISA slot that many high-end PCs no longer support.

The approach used in the design of the CVD was based on past success in hardware design and fabrication. A preliminary design was delivered to a consulting firm in order to produce an electrical interface design. Onboard logic for control of the electrical interface was then developed and prototyped. The logic established the theory of operation of the board, making it possible to test the concept using simulator software available from Lattice Semiconductors. With the interface and logic approved, a sound basis was available for deciding whether to proceed with the first build of the design.

Due to the checks and balances inherent in the design methodology, the rebuilds of the RSi4000RT and the CVD have been a complete success. Problems with earlier REV 1

versions of the RSI were corrected without any new problems arising. Likewise, very few electronic design problems were found in the new CVD boards. The most significant of these related to the circuit used for generating a synthetic antenna rate and was corrected by installing pull-up resistors on the input side of a CMOS inverter to convert the voltages to positive levels.

With the system components fully debugged, the new cards were integrated into the SeaScan (MRI) software previously developed by Sigma Engineering Limited in conjunction with the Transportation Development Centre of Transport Canada. The focus of the project shifted to characterizing the radar platform characteristics and evaluating the performance of the capture system. This involved that some laboratory tests be conducted in advance of the field-testing in Twillingate.

SOMMAIRE

La carte d'interface radar RSi4000 a été mise au point en 2001 pour améliorer la qualité des données et la performance de détection, lorsque jumelée au processeur radar SeaScan (autrefois désigné *interface modulaire radar*). Pour caractériser la performance de l'interface RSi4000, un programme de validation quantitative a eu lieu en 2002. Ce programme comprenait des essais en laboratoire de l'interface radar RSi4000 ainsi que des essais sur le terrain qui ont eu lieu en juin et juillet 2002 à Twillingate, Terre-Neuve.

En prévision des essais sur le terrain, des travaux ont été effectués sur le radar Raytheon Pathfinder MK2 pour corriger les problèmes qui s'étaient posés au cours des essais menés à bord du *Kometik* en 2000. Le radar a ensuite été installé sur le toit d'un fourgon modifié, aménagé de façon à offrir une plate-forme mobile permanente pour les présents essais et d'autres essais futurs.

Au cours de la phase intermédiaire du projet, Sigma a développé une nouvelle carte de décodeur vidéo composite (DVC) et l'a intégrée au système raccordé à l'antenne radar haute vitesse Raytheon MK2. Ce DVC extrait les données angulaires et les données d'état du signal vidéo et les convertit en un format compatible avec le RSi4000RT. Ce DVC a seulement besoin d'être alimenté par l'ordinateur, à la différence de la version antérieure, qui nécessitait une fente ISA, devenue à peu près inexistante dans les PC haut de gamme.

Pour la conception du DVC, les chercheurs ont utilisé une démarche qui avait fait ses preuves par le passé. Ainsi, une étude d'avant-projet sommaire a été remise à une firme de consultants avec le mandat de produire une interface électrique. On a ensuite développé et prototypé une logique de commande embarquée de l'interface électrique. La logique établissait le principe de fonctionnement de la carte, ce qui a permis de valider ce principe à l'aide d'un logiciel de simulation obtenu auprès de Lattice Semiconductors. L'interface et la logique étant validées, on disposait alors d'une base

solide pour décider de réaliser ou non la première version du concept.

Grâce aux autocontrôles intégrés, les nouvelles versions de la carte RSi4000RT et du DVC se sont révélées un succès complet. Les problèmes associés aux premières versions REV 1 de la carte RSI ont été facilement corrigés. Les nouvelles cartes DVC ont elles aussi posé très peu de problèmes de conception électronique, le plus important étant relié au circuit utilisé pour générer une cadence d'antenne dynamique. La correction a consisté à installer des résistances d'excursion haute du côté entrée d'un onduleur CMOS pour convertir les tensions à des niveaux positifs.

Une fois les composants du système mis au point, les nouvelles cartes ont été intégrées au logiciel SeaScan (IMR) qui avait été développé par Sigma Engineering Limited en collaboration avec le Centre de développement des transports de Transports Canada. Les chercheurs se sont alors attachés à définir les caractéristiques de la plate-forme radar et à évaluer la performance du système de saisie. Pour cela, il a fallu réaliser des essais en laboratoire avant de passer aux essais sur le terrain à Twillingate.

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GLOSSARY OF ACRONYMS

ACP	Azimuth Count Pulse
ADC	Analog-to-Digital Converter
ARP	Azimuth Reset Pulse
BIOS	Basic Input Output System
CFAR	Constant False Alarm Rate
CMC	CMC Electronics Inc.
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Complex PLD
CVD	Composite Video Decoder
dBFS	Decibels Full Scale
DIWAR	Direction Waverider Receiver
DLL	Dynamic Link Library
DMA	Direct Memory Accress
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
GB	Gigabyte
GPS	Global Positioning System
I/O	Input/Output
ISA	Industry Standard Architecture
LAN	Local Area Network
MB/s	Megabytes per Second
Mbps	Megabits per Second
MHT	Multiple Hypothesis Tracker
MRI	Modular Radar Interface
MSPS	Million Samples Per Second
nmi	Nautical Miles
PC	Personal Computer
PCB	Printed Circuit Board
PCI	Computer Bus Type
PLCC	Plastic Leaded Chip Carrier
PLD	Programmable Logic Device
PRF	Pulse Repetition Frequency
PROM	Programmable Read-only Memory
RAM	Random Access Memory
RMS	Root Mean Square
RPM	Rotations Per Minute
RSi4000	Radar Interface Card
SINAD	Signal-to-Noise and Distortion
SNR	Signal-to-Noise Ratio
TDC	Transportation Development Centre

1 INTRODUCTION

The Transportation Development Centre (TDC) of Transport Canada is involved in a variety of projects aimed at developing techniques and systems to enhance the small target detection capability of radar for use in Search and Rescue and iceberg detection.

Sigma Engineering Limited has developed a number of commercial products that enhance radar images through the use of high-speed scanners and high-definition digital acquisition. In cooperation with TDC, the company has produced a new generation of radar capture cards that combine the high bandwidth of the PCI interface with the high-definition of a 12-bit A/D chip. The resulting product is marketed by the company under the name of RSi4000-RT-8/12.

The RSi4000-RT-8/12 product is the result of more than 10 years' experience in the field of radar capture. It combines all the interface circuitry required to digitize images from most commercial radar in a single PCI-bus card.

The objective of the current activity is to characterize the new RSi4000 interface card, determining its full compatibility with the original design objectives while comparing its performance to the older interface card. In particular, the ability of the card to digitize in 12-bit resolution has the potential to greatly improve the performance of the Raytheon AI Tracker developed by TDC through other initiatives.

2 BACKGROUND

Advances in radar capture hardware now permit radar video from radar to be viewed in real time on a personal computer (PC). These digital radar images can be processed and enhanced by advanced software under the control of an operator. This capability significantly improves the ability to use radar for detecting nearby and distant objects in all weather and sea conditions.

With over 10 years' experience in the development of software for enhanced radar detection, Sigma Engineering Limited has relied upon many radar capture products, all of which were limited to 8-bit resolution. Technology has now advanced beyond past capacities; processing techniques can make use of higher resolution video to improve the signal-to-noise ratio of radar. To this end, Sigma Engineering developed the RSi4000-RT-8/12 (REV1), a straightforward, radar-specific capture card that supports up to 12 bits of digital resolution.

With the availability of the new 12-bit system, it became necessary to schedule field trials to evaluate the benefits of the higher resolution for detecting icebergs, bergy bits and pack ice. Several tasks were identified in preparation for this goal. These tasks were divided into five categories and are discussed in more detail in the following chapters:

- Preparing for system characterization
  - Repairing the high-speed scanner
  - Producing Rev 2 hardware
  - Outfitting a mobile platform
- Designing and building the CVD
- Supporting the Raytheon Canada MHT tracker
- Performing laboratory measurements
- Conducting field trials

3 PREPARATION FOR SYSTEM CHARACTERIZATION

This section describes the tasks required in order to prepare for system characterization.

3.1 Repairs to the High-Speed Scanner

Initially, damage to the electrical system that occurred as a result of the last shipboard trial on board the vessel Kometik was repaired. This damage resulted from the impact of excessive startup current on the inadequate cabling inside the radar unit. Cabling and interconnections were upgraded/repaired to withstand the increased startup current associated with the modified radar antenna's high speed.

Another problem identified in the Kometik trial was the slight misalignment of radar echoes from one scan to the next. This was related to poor tolerances of the mechanical gear system controlling the antenna. The radar was shipped back to TDC and modifications were conducted on the gear system in order to bring alignment within acceptable tolerance levels.

The radar was then delivered to CMC (CMC Electronics Inc.) where general maintenance, cleanup and inspection of the radar unit were performed. The "transceiver up" design of the radar limited the type of output power measurements that could be conducted. A visual test to confirm that the transmitter was functional was made by using the generated field to induce current in a light bulb filament.

The radar was allowed to run for an extended period of time, and it was found that the chassis of the radar was reaching a high enough temperature to potentially damage the electrical components inside. The radar was sent back to TDC where the lubrication was drained. Some metal filings were found in the extracted lubrication, but it was not clear whether these were the cause of the overheating or an effect. The antenna housing was thoroughly cleaned, fresh lubrication was installed and radiator fins were mounted to the chassis to draw heat away from the sensitive electrical components.

3.2 Production of REV2 Hardware

A number of recommended changes to the REV1 hardware were detailed in the Final Report of the Kometik trials. Since these involved relatively minor changes to the board layout that could potentially improve the video quality of the card as well as the ease of manufacture of the card (and therefore the cost of the card), it was felt that these changes should be implemented prior to characterizing the system. The list of suggested changes was submitted to Consolidated Technologies (sub-contractor) which took responsibility for modifying the layout and delivering the new design to a manufacturer for production.

3.3 Outfitting a Mobile Radar Platform

To facilitate long-term testing of the radar capture system, a cube van was outfitted to accommodate a roof-top transceiver. The van had to comfortably accommodate three people with related computer equipment.

Ranger Design, of Quebec, was able to provide a vehicle and the necessary modifications under the supervision of Charles Gautier and James D. Reid from TDC. The vehicle was shipped to Newfoundland aboard an OCEANEX container ship. Some additional work on the vehicle's suspension system was performed in St. John's.

With these preparatory modifications made, the van was delivered to CMC. At this point, several tasks remained to prepare the van for use, including:

- Installing a rack for storage of the computer equipment
- Running cables as needed for communications and connecting to the radar
- Securing the radar onto a metal plate
- Mounting the radar atop the vehicle

It had been intended to locate the computer rack on the generator housing; however, concern about the strength of the housing and access to the unit required that a new location for the unit be identified. One of the rear seats of the van was removed to accommodate the rack instead.

The computer that was purchased for the field trial was installed into the rack at this time.

4 DESIGNING THE CVD

Early testing showed that the memory speed of Pentium III class systems presents a bottleneck for processing and data distribution for the 120 RPM rotation speed at 12 bits. It was therefore necessary to purchase capture and playback hardware that supports new high-speed memory such as PC800 (RAMBUS) or PC2100 (DDR-266). Unfortunately, the chipsets that support these memory configurations do not support the ISA bus. Since the CVD, a 2-layer card that receives power from the ISA bus, is an integral part of the Raytheon MK2 high-speed scanner system, it was necessary to upgrade the CVD to a PCI form-factor to support the research activity.

The approach used in the design of the CVD was based on past success in hardware design and fabrication. From the outset, it was understood that the schematic design and PCB layout of the board would be done in close consultation with the electronics design contractor, Consolidated Technologies. This process required that a preliminary design be delivered to the contractor. After a review of the preliminary design, an electrical interface would be designed by the contractor that would meet the input and output specifications. Sigma Engineering Limited would then take full responsibility for developing the on-board logic. Once the logic was developed, the full schematics and PCB layout would be developed by the contractor. These would once again be reviewed before sending the files off for fabrication. Testing of the board would be done by Sigma Engineering Limited, with the contractor assisting in making modifications as required.

4.1 Conceptual Design

Since the CVD was based on a preexisting design of which both Sigma Engineering Limited and the contractor Consolidated Technologies Limited had detailed knowledge, the conceptual design phase was not required for this project.

4.2 Preliminary Design

The preliminary design was developed at an early meeting with Consolidated Technologies Limited. The preliminary design specified the following:

- Extraction of trigger and data from incoming composite video
- Placement of azimuth data onto RSi4000-RT compatible header
- Generation of serial RS-232 I/O messages for reporting status to the host PC
- Electrical conversion of RS-232 to RS-422 for sending data to the radar uplink
- Routing of video and trigger onto RSi4000-RT compatible cable
- Optional generation of ACP/ARP for complete control of RSi4000
- Generation of simulated video

4.3 Electrical Interface

In response to the preliminary design, Consolidated Technologies reviewed the available chips and quickly responded with electrical interfaces to the following components of the preliminary design:

- Two bidirectional channels of RS-422 I/O
- Two full-duplex RS-232 I/O
- 1.8432 MHz clock for baud rate generation
- 4 MHz clock for sampling of data from the composite stream
- Comparators with adjustable thresholds for detection of trigger and data
- Optional sine wave generator for ACP, ARP and video simulation

4.4 Logic Synthesis

With the electrical interface proposed, the focus shifted to prototyping the required PLD firmware. The firmware was developed using the ispLever software available from Lattice Semiconductors. The ispM4A series of CPLDs was chosen for implementation of the logic. These chips had all of the following features, which made them ideal for use in this project:

- Programmable without expensive hardware using a JTAG interface
- Programming software with support for the ABEL and Verilog languages available at low cost from Lattice
- Sophisticated simulation tools included in the Lattice software, allowing the logic to be fully tested during development
- Available with up to 256 macrocells allowing internal storage of 256 bits of data
- Low-cost, especially the ispM4A5-64/32-10JC

With the selection of the ispM4A5 as the target device, the layout required for the board's logic quickly took shape. Specifically, each of the required outputs was assigned to pins of the ispM4A5 devices. The remaining pins were used as control lines and handshaking between the various PLDs in order that three PLDs working in series could make the most effective use of the storage represented by the sum of their macrocells. The final implementation required three PLDs working in series to:

- Receive trigger and data
- Store the data bits and extract the angle information
- Generate an RS-232 serial message stream from the downlink data
- Generate an RS-422 serial message from the received RS-232 data
- Program the sine wave generator and baud rate based on switch settings
- Detect changes in the current switch settings
- Avoid timing violations among these signals

Due to the storage requirement needed to process the incoming and outgoing data streams, the PLDs could not be programmed incrementally. Likewise, they could not be easily tested within the limits of the ABEL programming language. Consequently, it was necessary to develop the firmware for the CVD using the Verilog programming language, which allowed a much more sophisticated simulation of the firmware than was possible using ABEL test vectors.

4.5 Schematic Design and PCB Layout

The pinouts for the three PLDs required by the design were provided to Consolidated Technologies Limited, which then added these to the design along with a JTAG interface. Schematics were then developed and the final design was reviewed by Sigma Engineering Limited. The schematics were approved with only minor revisions, and work was undertaken to position the components and traces on a PCI PCB layout.

4.6 Fabrication

The PCB layout files were sent to a manufacturer in order to generate the PCI card. After passing an electrical connection test at the factory, the board was delivered to Consolidated Technologies where the components were stuffed and mounted. The resulting card was then inspected and tested by staff at Sigma Engineering.

4.7 Initial Inspection

The fabricated board is a half-length PCI card with 5 V analog and digital power supplies derived from the host PC. The board is populated with all of the components on the top layer. The only through-hole component is the optional sine wave generator (U16). Interfaces to external signals are provided through a variety of connectors:

- A BNC connector (J1) supports access to the composite video source.
- A high-density DB15 connector (J2) is compatible with the RSi4000RT and provides pins for positive and negative sides of the ACP, ARP, trigger and video.
- A standard DB15 connector (J3) provides access to RS-232 and RS-422 I/Os.
- Header P1 provides a parallel azimuth word compatible with the RSI4000RT or common synchro-to-digital interfaces.
- Header P2 provides the interface to the JTAG cable used to program the onboard PLDs.
- Testpoints are available for examining ground, Vdd, Vee, trigger, data, and comparator thresholds.
- Various jumpers and switches control the direction, and baud rates of the serial, parallel and digital signals.

Initial inspection of the board involved examining the placement of device footprints, continuity between various ground points, as well as for Vcc, Vdd, and Vee, incorrectly

stuffed components and overall quality of the fabrication. When satisfied that the board power supply was safely assembled and that no defects were detectable, the board was installed in a PC via a bus extender card for initial power-up. The voltage levels on each of the power supply lines were verified and the card was watched closely to check for failing components.

4.8 Initial PLD Programming

The board was brought to Sigma Engineering Limited in order to program the PLDs and further test the card. The first step in the programming of the PLDs was to verify the presence and type of each device in the chain. Due to the storage requirement needed to process the incoming and outgoing data streams, the PLDs could not be programmed incrementally. The full firmware was downloaded to the board and the testing was conducted in stages. Specifically, the board was tested for the following behaviour:

- Detect changes in switch settings and respond by programming the sine wave generator and the baud rate
- Detect incoming data and respond by generating an RS-232 status message
- Detect incoming RS232 and respond by generating RS-422
- Detect triggers and respond by latching data onto the parallel header

4.9 Analog Analysis and Final PLD Programming

With the CVD functional, it was now possible to verify the actual operation of the board without the simulator. It was found that the sine wave generator was not behaving as expected. The problem was traced to the fact that its negative going output was connected to a CMOS inverter. The solution was to raise the voltage being applied to the inverter input by 2.5 V using a resistor pull-up configuration.

When connected to the actual radar, it was found that the sampling of the data occurred too close to the transition zones. An adjustment to the baud rate generation firmware was made to correct this. No other problems of a significant nature were found.

5 SUPPORTING THE RAYTHEON CANADA MHT

The Multiple Hypothesis Tracker (MHT), developed by Raytheon Canada, was designed to operate in conjunction with the SeaScan system. As part of this project, the MHT was upgraded to support the high resolution data format. The new MHT supports both 8 and 12-bit modes. A report produced by Raytheon Canada documenting this upgrade is included in Appendix D.

One version of the SeaScan system included special functions to support optimum performance of the MHT. However, these functions were not in the main stream of system maintenance and upgrades. As part of this project, these functions were incorporated into the main SeaScan product line. The result is a single product that fully supports the MHT.

6 LABORATORY MEASUREMENTS

System characterization occurred in two parts. The first class of tests are independent of the platform and were conducted in a laboratory environment:

- Data acquisition signal-to-noise ratio for old and new cards
- Data recording scope (range and sector) and throughput
- Mobile platform stability

Due to the choice of a transceiver-up design for the radar, it was not feasible to conduct the following tests, especially in light of the fact that specifications for these values were readily available from the radar manufacturer:

- Radar system output power level
- Radar system signal-to-noise ratio
- Radar performance against injected targets

Each laboratory measurement will have a concise test plan with the following format:

- Objective
- Measurement Theory
- Acceptable Tolerances
- Required Instrumentation and Signal Generators
- Test Setup
- Measurements
- Analysis

6.1 Signal-to-Noise Ratio Measurements

6.1.1 Objective

To measure the signal-to-noise ratio (SNR) and the effective number of bits (ENOB) for the new data acquisition card (RSi4000RT).

6.1.2 Measurement Theory

Measurement theory for this procedure is given in Appendix B.

6.1.3 Acceptable Tolerances

The manufacturer of the ADC (analog-to-digital converter) rates the 12-bit device as having an SNR of 68 dB. Since an ideal 12-bit ADC yields an SNR of 74 dB, achieving an ENOB of 12 bits is unrealistic, and an ENOB of 11 bits would indicate an exceptional implementation. The test equipment and processes used for measuring and computing the SNR have to be of sufficient quality so as not to compromise the 68 dB goal.

6.1.4 Required Instrumentation and Software

To generate the required test signals for the SNR measurement, a high-quality signal generator with true 12-bit resolution was required. For maximum control over the test inputs, the signal generator should have the ability to download an arbitrary waveform from 12-bit data, and output it at sampling rates comparable to those of the RSi4000RT (maximum rate 60 MHz).

The HP33120A 40 MSPS arbitrary waveform generator was determined to be a good choice for the signal generator. It accepts 12-bit waveforms up to 16,000 samples, and has built-in capability to interpolate and reformat the waveform to generate a signal with a bandwidth as high as 15 MHz. A burst-mode capability allows the signal to be associated with a synchronization trigger marking the start of video generation.

Also required for the test is a spreadsheet application for computing the Fast Fourier Transform (FFT) of the captured waveform. Microsoft Excel can process an FFT of up to 4,096 points. This was deemed adequate for the required measurements; consequently, Microsoft Excel was selected for the analysis.

6.1.5 Measurements

Figure 1 shows the frequency spectrum (phasor amplitude) for the original prototype card when tested according to the test procedure described in section 6. In the center of the graph is the dc component at 6 dBFS, situated between the two fundamental signal components at -0.5 dBFS. The noise floor sits just above the -90 dBFS marker, and two noise spikes of -72 dBFS amplitude appear at +/-6.088867 MHz.

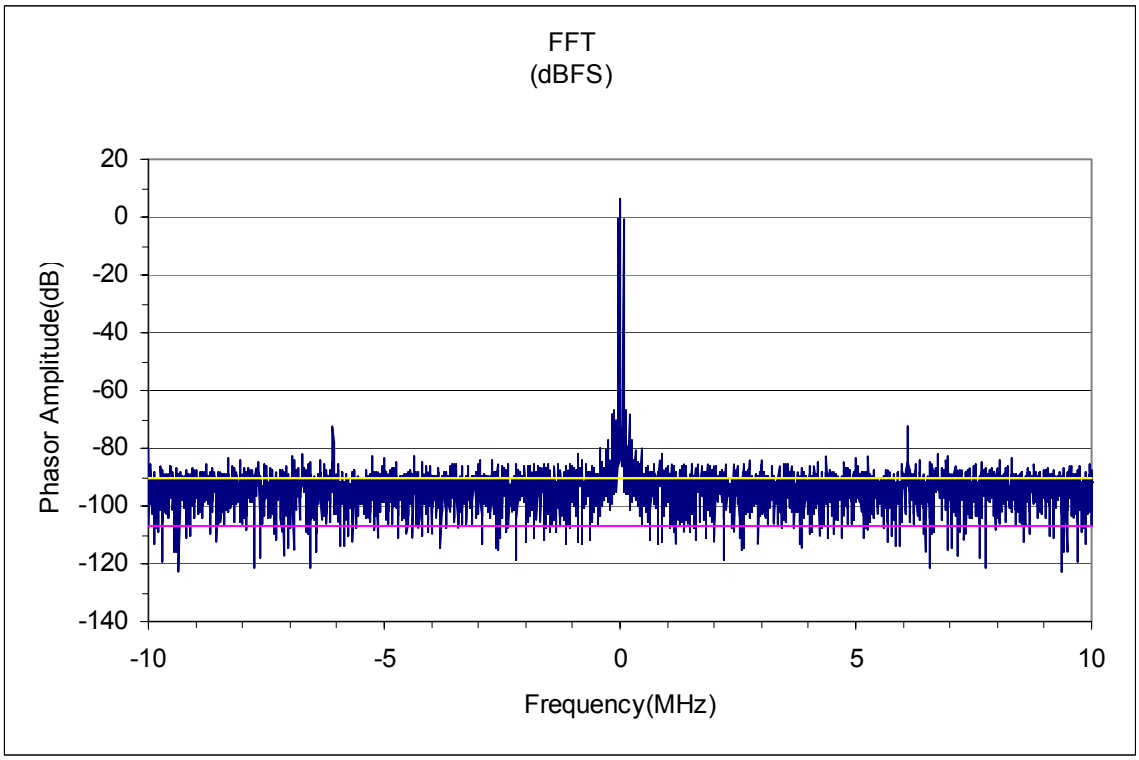


Figure 1. Spectrum for Prototype Card (20 MHz Sampling, 4,096 levels)

Two ratios for the prototype card were computed: the first (SNR) weighted the signal and harmonics against the noise background; the second (SINAD) accounted for some distortion by including the sidelobes of each harmonic as part of the signal. The values

for each are given in Table 1.

Table 1 SNR and SINAD for Prototype

	dBFS	Noise Floor (dBFS)	ENOB
SNR	57	-91.4	9.2
SINAD	59	-92.9	9.5

The REV2 card was built, and a review of the ADC front end was conducted. The review brought to light the relationship between the as-configured maximum gain of the video pre-amplifier, the maximum allowable video voltage, and the resulting bandwidth of the amplified video. It was determined that when the REV1 was configured for maximum gain and subjected to a maximum input voltage, the amplifier bandwidth was in an undefined region of operation. To correct this situation, the maximum voltage presentable to the amplifier was changed to 2.7 V, and the front end voltage divisor was changed from 2:1 to 3:1. The maximum gain on the amplifier was set to 3 to allow low voltage signals to be recovered. With these changes, the bandwidth of the amplifier is expected to be approximately 100 MHz. Other changes to the REV2 card included better grounding and better isolation of analog and digital signals.

Figure 2 shows the frequency spectrum (phasor amplitude) for the REV2 card when tested according to the test procedure described in the section 6. In the centre of the graph is the dc component at 6 dBFS, situated between the two fundamental signal components at -0.5 dBFS. The noise floor sits just below the -90 dBFS marker, and noise spikes do not rise above -80 dBFS amplitude.

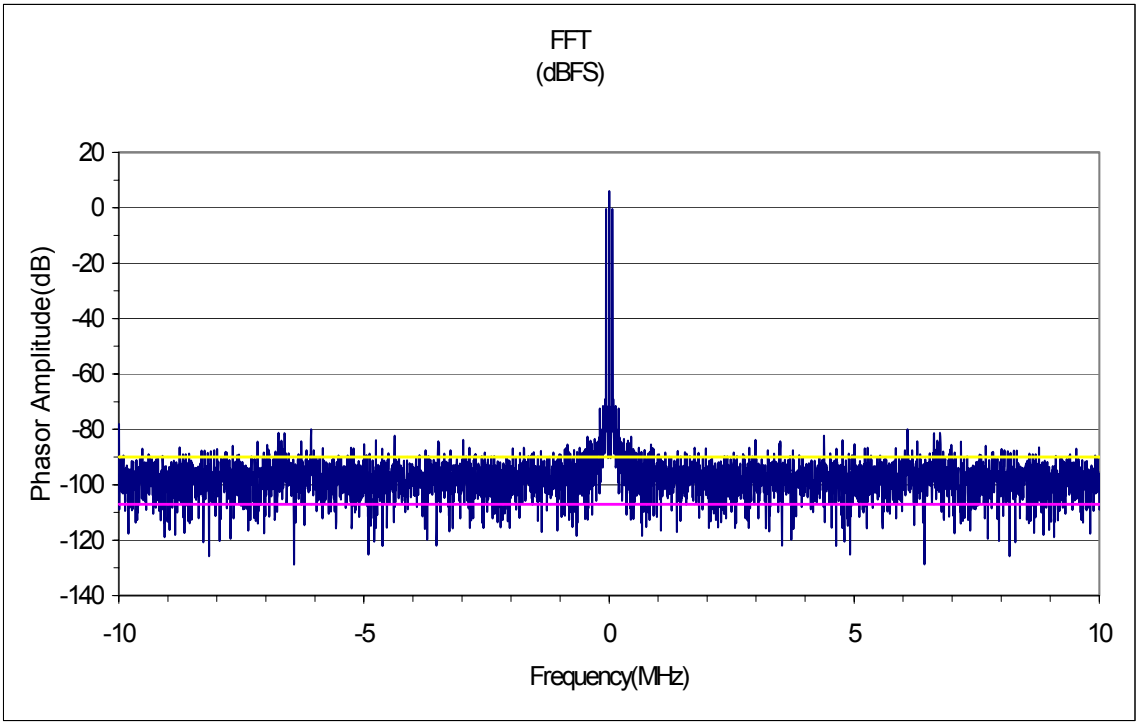


Figure 2. Spectrum of REV2 Card (20 MHz Sampling, 4,096 levels)

Two ratios for the REV2 card were computed: the first (SNR) weighted the signal and harmonics against the noise background; the second (SINAD) accounted for some distortion by including the sidelobes of each harmonic as part of the signal. The values for each are given in Table 2.

Table 2 SNR and SINAD for REV2 Card

	dBFS	Noise Floor (dBFS)	ENOB
SNR	59	-93.0	9.6
SINAD	61	-94.7	9.9

Due to the fact that the signal generator being used was 12-bit, some concern was expressed that the 12-bit quantization of the source signal was limiting the performance of the system. The limit was not so much a question of resolution as it was a question of scale. The signal generator was able to output incremental voltage differences as small as 12 μV, which provides quite a good resolution when compared to the 488 μV per bit of resolution for which the ADC is configured. Unfortunately, the full 2 V range of the ADC can only be realized by compromising the resolution of the signal generator.

To avert this problem, equations used for SNR and ENOB incorporated the ability to accommodate less than full-scale signals. Measurements were taken with the full-scale output of the generator halved and quartered, and the SNR and ENOB computed based on the percent of full-scale voltage exercised by the test. Figures 3 and 4 summarize the results of this test.

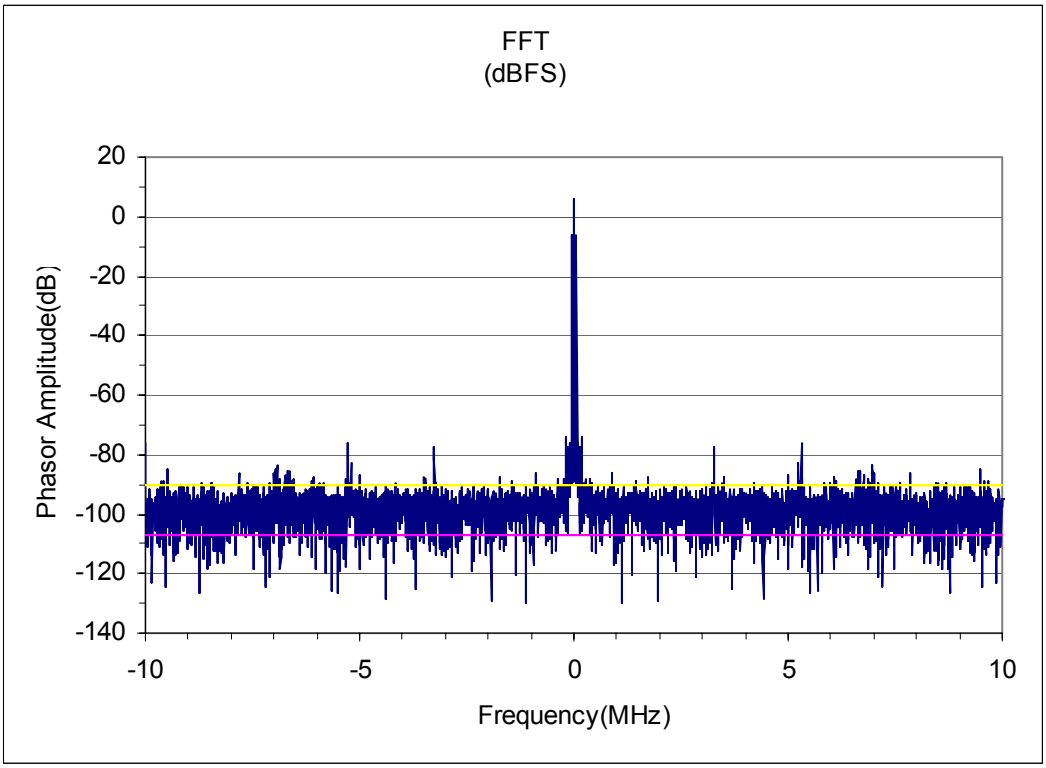


Figure 3. Spectrum of REV2 Card (20 MHz, 2,056 digital levels of 4,096)

Two ratios for the REV2 card with half amplitude input were computed: the first (SNR) weighted the signal and harmonics against the noise background; the second (SINAD) accounted for some distortion by including the sidelobes of each harmonic as part of the signal. The values for each are given in Table 3.

Table 3 SNR and SINAD for Half Amplitude Input

	dBFS	Noise Floor (dBFS)	ENOB
SNR	55	-93.9	9.8
SINAD	56	-95.6	10.1

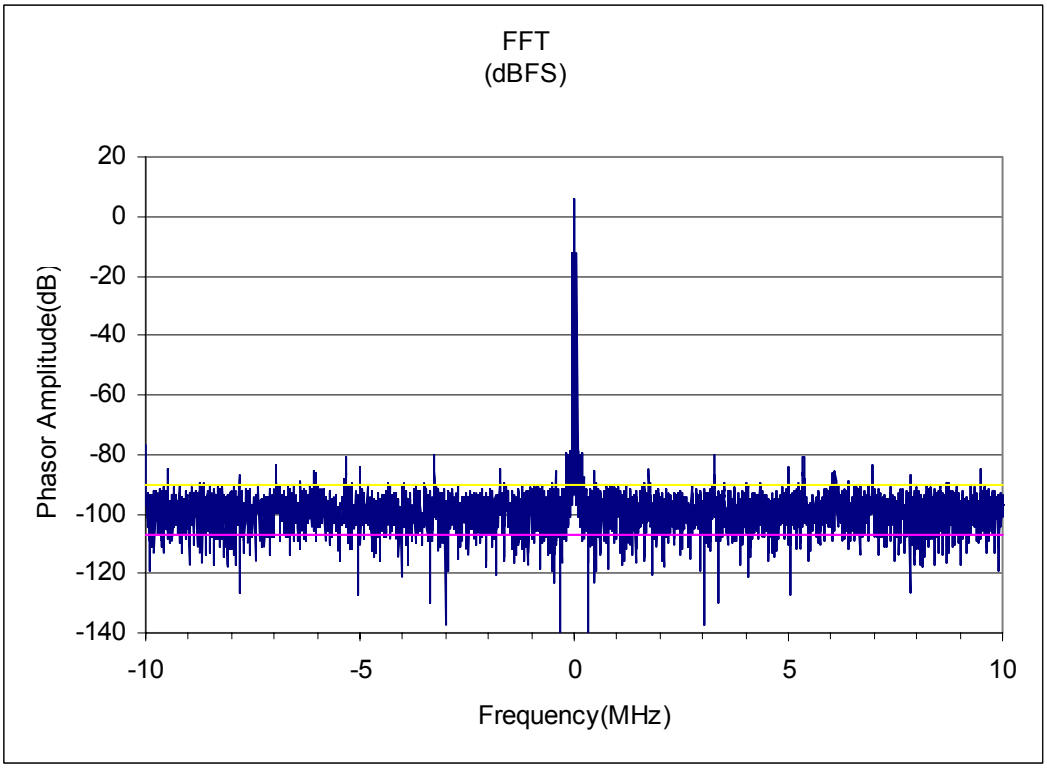


Figure 4. Spectrum of REV2 Card (20 MHz, 1,030 digital levels of 4096)

Table 4 shows that, for an input of quarter amplitude, there is a further improvement in ENOB.

Table 4 SNR and SINAD for Quarter Amplitude Input

	dBFS	Noise Floor (dBFS)	ENOB
SNR	51	-95.9	10.1
SINAD	52	-97.0	10.3

Reducing the voltage below 586 mVp-p (Quarter Amplitude) offers no additional improvement in the effective number of bits.

6.1.6 Signal Processing Gain

In order to investigate the effect of signal processing on the effective number of bits, the sampled data was averaged over 32 consecutive pulses. This type of processing is currently used in the radar processor to improve the target signal-to-noise ratio. Figure 5 shows the spectrum of the averaged data.

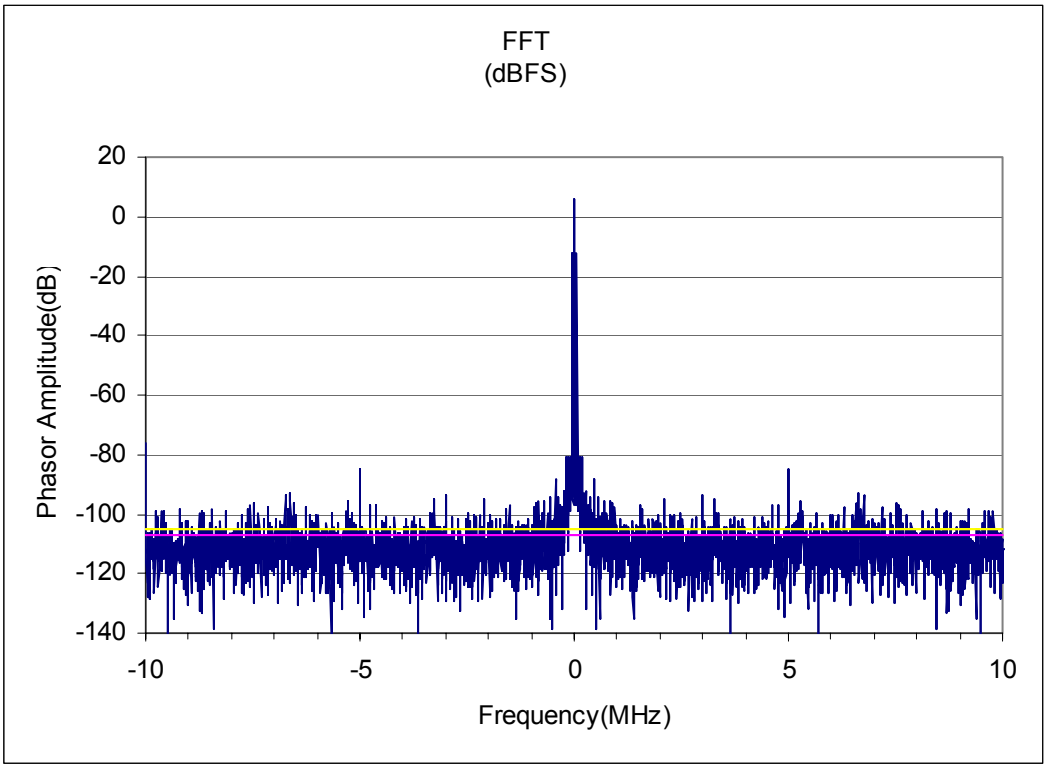


Figure 5. Spectrum of REV2 Card (20 MHz, 32 pulses averaged, 1,030)

Table 5 presents the measurements for 32 pulses averaged. This is equivalent to pulse filter processing in real-time operation.

Table 5 SNR and SINAD for 32 Pulses Averaged

	dBFS	Noise Floor (dBFS)	ENOB
SNR	55.5	-100.7	10.9
SINAD	60	-105.1	11.7

The processing of 32 pulses of data provides an ENOB of 11.7. When we add back the 12 dB reduction in input signal, the system SNR would be 67.5 dB and SINAD would be 72 dB – very close to the theoretical limit of 74 dB for a 12-bit converter. This is an excellent result and indicates that, for typical radar signal processing processes like pulse to pulse and scan to scan integration, the new RSi4000 will provide close to 12-bit resolution.

6.1.7 Analysis

In order to better characterize the factors that affect the SNR of the card, a number of experiments were conducted on the REV2 card. The first experiment was to determine the range of gain provided by the newly configured amplifier. This was determined by repeating the FFT for the REV2 card and dropping with the gain from its previous value of 255 to 1. We would expect the total power of the signal to drop by 20*log(1/255) = - 48 dB when the gain is set to 1. As Figure 6 shows, each of the sinusoidal components resides 3 dB below this value, confirming that the total combined power is the 48 dB result.

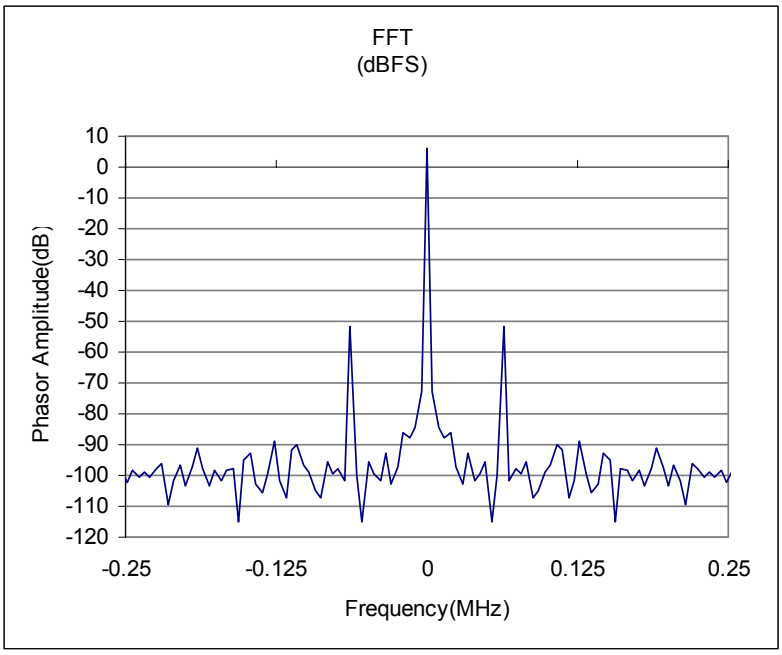


Figure 6. Spectrum with a Gain of 1 and a 2.574 V Sine Wave

The next experiment was to determine the effect of increasing the voltage of the signal generator. This was done by leaving the gain setting at 1 and increasing the video from 2.574 Vp-p to 5.0 Vp-p with an offset of +2.5 Vdc. The expected increase in signal strength would be 20*log(5.0/2.574) or approximately 6 dB. As Figure 7 shows, this was indeed the case.

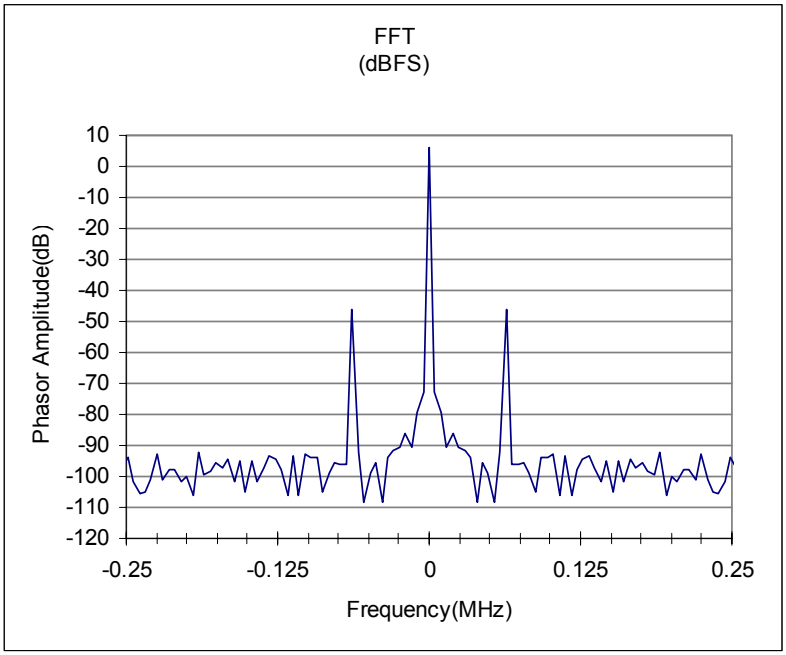


Figure 7. Spectrum for a Gain of 1; 5 V Sine Wave Input

A side effect of the increased voltage is that the flatness of the noise floor suffers beyond 5 MHz. This can be seen in Figure 8. To determine whether the source of the noise was internal to the card or coming from the signal generator, the signal was divided by two using an inline voltage divider circuit. Since this restored the flatness to its original level (see Figure 9), and in both cases the signal generator and the ADC were delivering and receiving identical voltages, the conclusion was drawn that the bandwidth of the front-end gain amplifier was being affected by the increased voltage.

The 5 MHz boundary probably relates to the percentage of the sinusoidal duty cycle where the voltage is high enough to enter a non-linear region of the amplifier. This saturation region is of trivial interest in most radar applications. In the rare case when a high percentage of radar video is beyond the 5 V range, some performance gain can be realized by passing the video through a passive 2:1 attenuator before connecting it to the RSi.

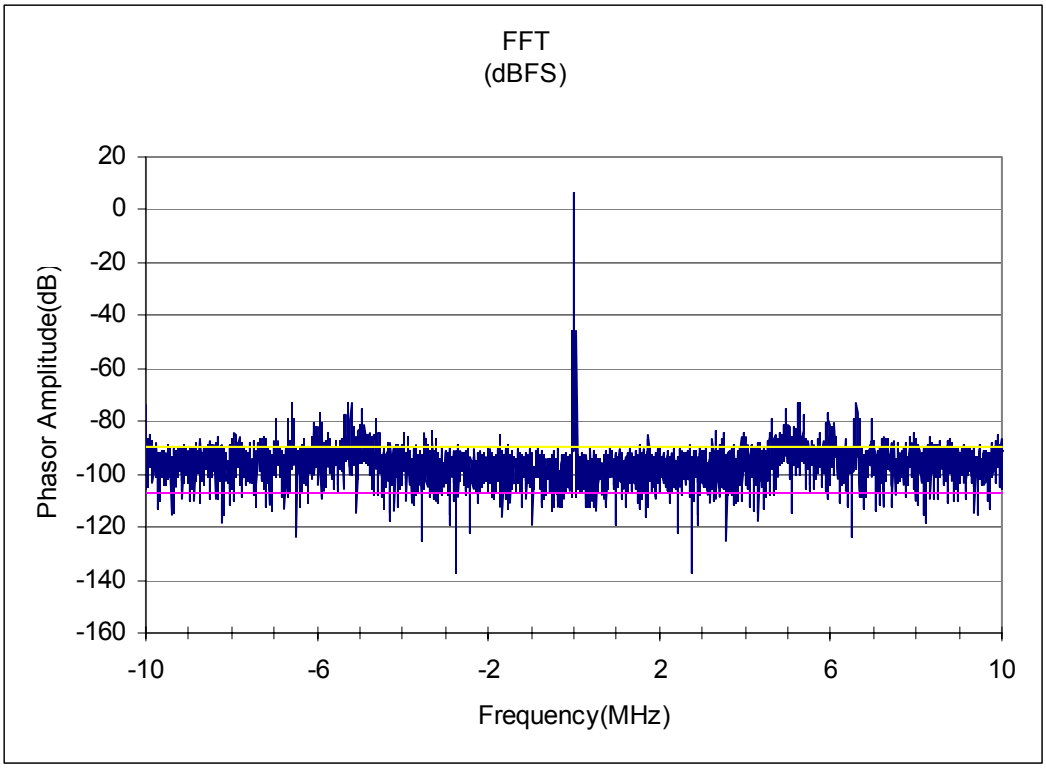


Figure 8. Spectrum for a Gain of 1; 5 V Sine Wave (10 MHz)

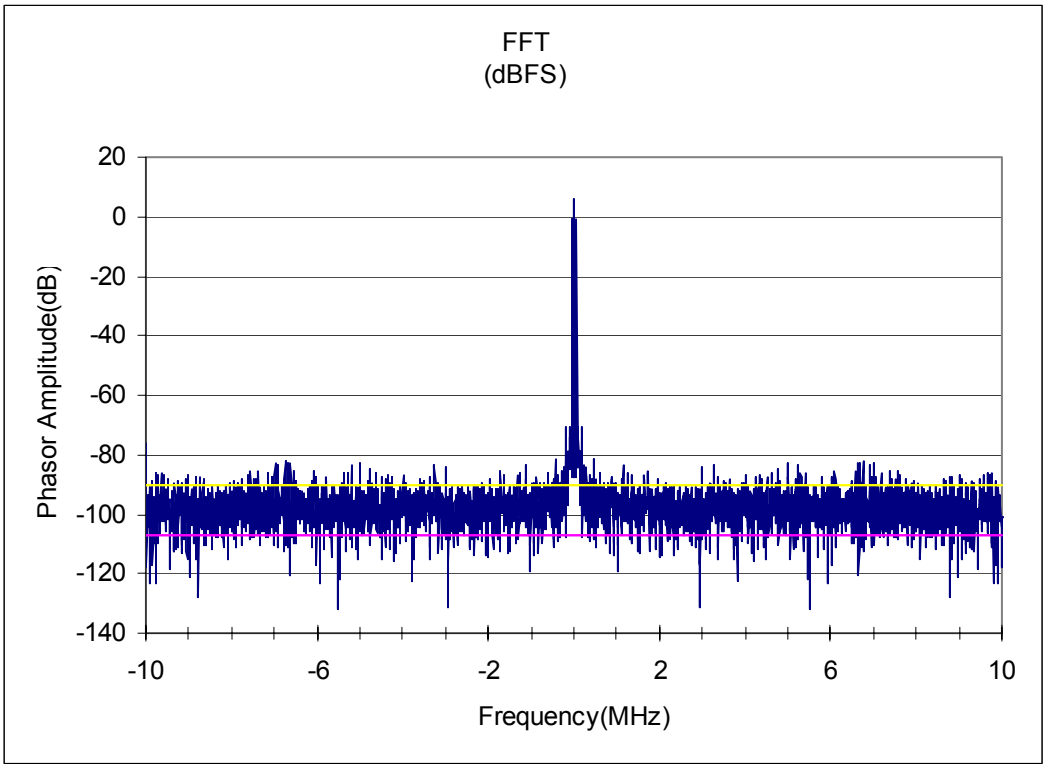


Figure 9. Spectrum for a Gain of 1; 5 V Sine Wave with Voltage Divider (10 MHz)

6.2 Data Recording Scope (Range and Sector) and System Throughput

6.2.1 Objective

To measure the throughput of the system, both for live capture and also for data recording.

6.2.2 Measurement Theory

To measure data recording scope and throughput, the host platform is first configured to match the configuration to be used during field testing. It is important that all potential interactions between BIOS settings, hardware, drivers, operating system and software be identified and resolved prior to making measurements.

6.2.3 Upgrade to Device Driver

The higher throughput possible using Pentium IV Xeon processors and PC-800 memory taxed the RSi4000RT device driver beyond the limits of the previous platform. Modifications were made to the way in which the driver disabled bus-master transfers in order to prevent data corruption and eliminate unwanted interrupts.

6.2.4 Acceptable Tolerances

The measurements described in this section are to be based on system throughput using release versions of the system software. Throughput must be maintainable in the presence of reasonable levels of user activity such as task switching and disk access.

6.2.5 Measurements

6.2.5.1 System Throughput Testing

The throughput of the SeaScan system was measured on one of the PCs acquired for the field trial. This PC contained a motherboard with Dual Pentium 4 XEON processors running at 2.0 GHz. The system was equipped with 1 GB of RDRAM.

A radar simulator test bed was used to generate the required signals. This simulator was configured as a 60 RPM scanner, with an ACP count of 4,096. The system was configured to collect 2,048 samples at 40 MHz, and to produce a gated image with 4,096 pulses. The sample depth was 12 bits.

The system was started with a PRF of 4 kHz. Only basic processing (scan conversion and scan averaging) was performed. A display client was used to verify the proper formatting and delivery of the data.

The PRF was increased until the RSi4000 trigger status LED began to flash, indicating that the system was not able to keep up with the input data rate. The maximum PRF at which data was able to be captured continuously without loss was 13.7 kHz. This corresponds to a data capture rate of 56 MB/s (million bytes per second) computed as 2,048 samples x 13,700 Hz x 2 bytes per sample.

The system was also able to perform pulse filtering at this data rate without dropping any data.

The data simulator was reconfigured to generate the signals expected during the field trials, consisting of a 120 RPM scanner with an ACP count of 4,096. The system was configured to collect 4,096 samples at 40 MHz, and to produce a gated image with 1,024 pulses. The sample depth was 12 bits. During this testing, it was found that the CFAR algorithm was not able to keep up with the incoming data.

The implementation of the CFAR algorithm makes the CFAR processing time dependent on the data. Part of the algorithm stores data in an array whose length is

matched to the bit depth of the data. The more data is spread through this table (which is typical for radar data), the longer it takes the algorithm to run. The longer array required for 12-bit data increases the processing time.

The function of the CFAR routine is to remove any range dependency from the data by estimating the background level and subtracting it from the data. It was believed that a reasonable estimate of the background could be made using only the upper eight bits of the data sample.

This change was made to the CFAR routine. It was found that the speed was increased by a factor of two. The CFAR routine now takes the same amount of time for both eight- and twelve-bit modes.

6.2.5.2 Tape Testing

The tape drive used in previous field trials was the Exabyte Mammoth. This tape drive had a measured maximum data rate of about 2.7 MB/s (nominally 3 MB/s). To support the increased data provided by the RSi4000 over the previous generation capture cards, new tape drives were acquired. The new capture card can collect as many as 4,096 samples per pulse in 12-bit mode. When used with the Raytheon MKII radar, the data rate can be as high as 24 MB/s. The maximum data rate provided by readily available tape drives is only 12 MB/s. Since the Exabyte drive had been used previously with good success, the tape drive chosen for this project was the Exabyte Mammoth 2.

In order to provide maximum flexibility, the drives were purchased as external, stand-alone units. The performance of the tape drive was measured using an existing benchmark program, which was modified to write more data to the tape to accommodate the increased throughput. The data transfer rate to the drive is data dependent, as the tape has built-in compression. In the case of totally random data, the maximum write speed was 10.9 MB/s and for totally flat data (all data values the same), the maximum write speed was 36.5 MB/s. Read speeds for the same data were slightly higher (11.3 and 37.8 MB/s, respectively).

Even with the new high-speed tape drives, the system would only be able to record about 165° at maximum range for short pulse data. When the RSi4000 is in 12-bit mode, data is actually transferred in 16-bit blocks, with the upper four bits being unused. The capability of repacking this data prior to recording was added to the storage module of the SeaScan server. This increased the collectable sector to about 215°.

6.2.5.3 Gigabit Network Testing

At the beginning of the project, it was uncertain whether a single PC could perform both the data capture / primary processing and the plot extraction processing. Therefore, it was decided to purchase a second PC to host the plot extraction system. Data would be transferred between the two systems over a network.

Data transfer rates over 100 Mbps links have typically been measured at about 6 MB/s. For this project, it was desired to collect 4,096 samples in short pulse mode (giving a maximum range of 8 nmi). For an image with 1,024 pulses, the resultant image size is 8 MB. For a real-time system with a 120 RPM scanner, the required network bandwidth is therefore 16 MB/s.

To achieve this, two Gigabit (1,000 Mbps) network adaptors were purchased. These cards have a 64-bit PCI connector for maximum throughput from the host PC memory.

Existing TCP/IP benchmark programs were used to measure the performance of these cards. Initial tests showed a maximum throughput of 33 MB/s. CPU usage on both the sending and receiving PCs was about 20%. However, it was discovered that the transfer rate was dependent on the block size used. This was eventually traced to a delay mechanism in the benchmark program. When this delay mechanism was removed, the system was able to transfer data at a rate of 65 MB/s. The CPU usage at this data rate was very high at 40% on the receiving PC and 75% on the sending PC.

Since the target bandwidth was 16 MB/s, and CPU usage is negligible at this data rate, it was concluded that these cards were acceptable and that it would be possible to run the plot extractor on a second PC.

6.2.6 Analysis

The capture hardware is able to transfer data at 56 MB/s, which is 81% of its theoretical maximum of 66 MB/s. The ability to process data captured at this rate is dependent on the memory speed of the host computer and the bit depth of the processed output. When used with the Raytheon MKII radar, the useful data rate is only as high as 24 MB/s meaning that capture and processing throughput is more than adequate for this application.

The recording and playback rate using tape is limited to 10.9 MB/s (assuming minimal hardware compression). This allows only 215° to be recorded per scan when capturing 4,096 samples in 12-bit mode using the Raytheon MK2 high-speed scanner.

Network throughputs using Gigabit LAN adapters were found to be 65 MB/s maximum. Not surprisingly, the 65 MB/s maximum achievable from the 1,000-Mbps adapters represents a 10-times increase over older 100-Mbps cards. Such rates unfortunately carry a hefty CPU usage penalty, monopolizing up to 75% of the processor time. More practical speeds of 16 MB/s represent a respectable improvement over the slower architectures and are easily realized over Gigabit LANs with negligible CPU usage.

6.3 Mobile Platform Stability

6.3.1 Objective

To measure the electrical and mechanical stability of the mobile platform.

6.3.2 Measurement Theory

Mechanical stability is related to the suspension system of the cube van. The horizontal beamwidth of the antenna also plays a factor. Electrical stability is related to the quality of the power generator, the quality of the PC power supply, and the load on the power supply, especially during startup of the radar.

6.3.3 Acceptable Tolerances

From the point of view of mechanical stability, the tolerances were quite large since the horizontal beamwidth of the antenna is 1 degree. Mechanical vibration on this order would be quite noticable and consequently quantitative measurements were not deemed to be necessary.

Experience with electrical stability has shown that significant problems with electrical stability can be measured qualitatively as well. Specifically, an excessive load on a generator during radar startup will cause an audible change in the generator motor's RPM and a drop in supply voltage. Excessive current through relays will produce a visible spark, and electrical power characteristics outside the specifications of a PC's power supply will cause the PC to reboot.

6.3.4 Required Instrumentation and Software

Due to the qualitative nature of the measurements, no special equipment was required for these tests.

6.3.5 Measurements

Initially, the van was loaded with the equipment expected to be installed during normal operations. The vehicle was road tested in order to determine its maneuverability.

A second vehicle monitored the motion of the van as it traveled. The conclusion was made that the suspension of the vehicle was weak for the load. The weak suspension

not only made driving difficult, it also threatened to cause some of the undercarriage to strike bottom on rough roads. The vehicle was taken to a local autobody shop to be outfitted with a “spring kit”.

The vehicle was then taken to CMC. The radar was connected to the generator of the van and started and stopped a number of times prior to installing the radar atop the vehicle. The generator appeared to have no problems delivering the necessary electrical power to radar. The relays installed in the radar demonstrated excessive startup currents resulting in electrical arching between the contacts.
A heavier gauge relay reduced the sparking but did not eliminate it entirely. The theory of generators and motors was reviewed. From this review, it was determined that motors and generators are related in their design, and that a motor that is disconnected from a power supply generates enough voltage to cause the effect being seen.
A capacitive load was put across the relay in order to accept the motor’s voltage when the power supply was disengaged.

The radar was then mounted on top of the vehicle and all the necessary equipment was installed inside the van. The radar was operated in order to determine whether the antenna rotation had any effect on the vehicle’s mechanical stability. It was found that the van’s geometry prevented yaw and pitch, but allowed a significant amount of roll when the antenna was turning. Stabilizer jacks installed on the van were lowered, and the test was repeated. With the stabilizer jacks in operation, no detectable motion was experienced.

6.3.6 Analysis

Upon final analysis, the mobile platform’s mechanical and electrical stability were found to be acceptable for field trials.

7 TWILLINGATE FIELD TRIAL

During June 2002 a comprehensive field trial was undertaken to validate the performance of the new RSi4000 and to collect a data set with the new card for assessment of the iceberg detection capability of the new system. Twillingate, Newfoundland, was selected for the trial. This site was selected as it was expected to provide sufficient iceberg targets for an effective evaluation of the system. The Twillingate site was used for a field trial in 1999 and so the logistics of using the site were well known.

In 2002 TDC acquired and modified a cube van for use in the radar validation and future data acquisition trials. The van was outfitted as a self-contained unit capable of operating in a cold weather climate. The unit was fitted with a 5 kW generator and electric heat.

7.1 Test Platform

Figure 10 shows the unit located at Twillingate, Newfoundland, overlooking the test site. The Raytheon Pathfinder MK2 is mounted on a prefabricated platform. The figure shows the heat sink mounted on the radar case to dissipate heat. During the trial no heating problems were noted so this configuration worked well. This radar had been specifically modified for radar research activities to operate at 120 RPM, almost five times the speed of the standard antenna. The main purpose of the high-speed antenna is to provide increased opportunities to detect growler and other small targets in high sea states. The principle behind the research is to investigate whether the increase in opportunities translates into an increase in detection performance.

The SeaScan system was equipped with recording capability for the trial in order to facilitate its evaluation. This permitted both in-field evaluation and post-field trial evaluation of the system. This was possible as the data recording capability provides full bandwidth raw radar data. This capability enables the re-creation of the exact situation as it occurred in the field and the application of different processing and tracking parameters. The tape units used for the trial were Exabyte M2 units capable of close to 12 MB/s continuous recording.

Figure 10. Mobile Radar Unit at Twillingate, Newfoundland

Figure 11 shows a view inside the van with the test setup. The radar processor is located in the rack unit at the far end of the table. The equipment at the right of the picture is the logging equipment for the wave and wind data.

Figure 11. Interior View of Mobile Radar Unit

7.2 Environmental Conditions

The main focus of the trial was to determine system detection performance on growlers and bergy bits in high sea states. In order to facilitate this and to maximize the probability of getting the desired data, an extended field trial was designed. Once the equipment was deployed at Long Point, Twillingate, conditions were monitored and field personnel mobilized when conditions were suitable for data collection. This mode of operation permitted leaving the equipment in the field for a six-week period.

Overall data was collected on numerous growler and bergy bit targets in sea states up to 3.5 m significant wave height (5.9 m maximum wave height) and wind speeds to 35 kn. Iceberg aerial ground truth data was collected by C-CORE and surface based ground truthing of iceberg targets was conducted by Sigma Engineering Limited and

Oceans Limited of St. John's. Oceans Limited also provided weather forecasting for the site and in-situ measurements of wind and wave data.

During the trial, radar data was collected on various sizes of icebergs ranging from growlers to very large icebergs. The data was collected during seven data collection days: June 5, 6, 14, 15, 16, 21, and 22. Oceans Limited was contracted to provide weather forecasting and ground truthing support for the trial. A comprehensive ground truth report was compiled by Oceans Limited and includes summaries of all environmental and iceberg data collected during the period. This report provides position information on icebergs that were observed visually from the surface and from aircraft.

Waves were measured using a non-directional Datawell waverider buoy that was moored in position 49° 43.06'N; 54° 47.56'W (018° True at two miles from the radar site). Data was collected and archived through a Digital Waverider Receiver (DIWAR) and laptop interface. Wind speed and direction were measured in the vicinity of the radar site at a height of 2 m above the surface using a RM Young anemometer. Wind data was collected and archived through a Campbell Scientific Datalogger and laptop interface. A hand-held anemometer (Skywatch Elite) was used as a backup and this unit also provided air temperature. Wind data from the Twillingate Lighthouse was also recorded on June 14, 15, 16, 21 and 22.

With the exception of June 16, icebergs were observed visually on each data collection day by Oceans Limited. On June 16 there was only one hour of radar data collection and during this period the visibility was only an 1/8 of a mile. Observations were typically taken every one to two hours. Visual observations were supported by photographs taken by Sigma Engineering Limited. These photographs were subsequently analyzed to confirm iceberg sizes. Additionally, three over flights were carried out by C-CORE. Information from these flights, which took place on June 5, 14 and 21, was also incorporated into the compilation of the iceberg data.

To support the project, five-day forecasts were issued daily by Oceans Limited. These forecasts were used for the planning of field trips and data collection events.

Table 6 Radar Site Characteristics

Latitude:	N49º 41.230'
Longitude:	W54º 48.206'
Height:	300 ft (91 m)
Radar Horizon:	21 nmi (39 km)

7.3 Example Data Summary

The complete field data set includes environmental and iceberg ground truth data. Iceberg photographs are available in digital form and have been archived on CD for use in detailed analysis. For the trials the bulk of the iceberg ground truthing photographs were taken using a Canon s40 digital camera. This four-megapixel camera has a three times optical zoom and records focal length with each picture so that absolute target measurements may be made during the analysis task. The camera was calibrated using a target at a measured distance and tested for the range of focal lengths available. A spreadsheet was constructed so that iceberg target pixel dimensions could be entered along with range and focal length, and dimensions would be automatically calculated.

This section summarizes an example of the data available for analysis. The data selected was on the day with the highest sea state (June 15). Unfortunately, visibility during the day was very poor so ground truthing photographs could not be taken until later in the day. This provided a very good opportunity to evaluate the operational capability of the system as field personnel were blind to the actual situation. Early in the morning a target was identified near a medium grounded iceberg at a range of 2.6 nmi. Visual confirmation of the target was not possible until later in the day but the target was tracked from 2.5 nmi into a range of about 0.8 nmi. At the near range the target entered into the shadow zone in front of the radar caused by terrain. The target was monitored intermittently as it moved through the shadow regions and at 0.6 nmi it was observed visually as a small bergy bit. A number of photographs were taken to document the target and to make size measurements.

A complete data summary is provided in the Oceans Limited ground truth report. Figures 12, 13 and 14 summarize the environmental conditions during the bergy bit data collection (June 15, 2002).

On June 15 a north-northwest to north wind prevailed during the first half of the radar data recording period. Then, about mid-period, the wind veered into the north-northeast. [**Note:** the R.M. Young anemometer located in the immediate vicinity of the radar site was observed to undergo erratic behaviour in turbulence eddies due to the influence of the local topography in the north-northeast winds. As a consequence, the quality of these data was very poor under these conditions.] Based on wind speeds recorded at the Twillingate Lighthouse weather station WDO combined with hand-held anemometer measurements, the wind speed over the water was estimated to be near 25 kn with gusts of 30 to possibly 35 kn early in the period. Winds of 15 to 20 kn prevailed in the north-northeast winds during the latter half of the recording period.

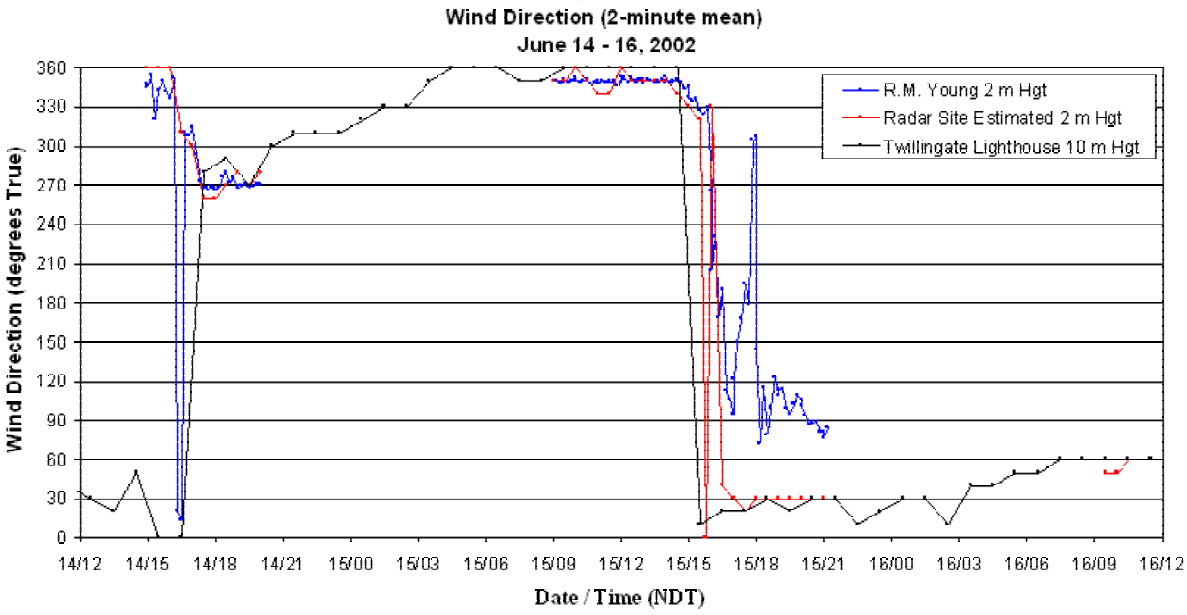


Figure 12. Wind Direction for June 14 to 16

The significant height of the combined seas ranged between about 2.9 m and 3.5 m during the data recording period, with an average zero-crossing period between 6 and 7 seconds. A maximum of wave height of 5.95 m was recorded during one 20-minute sampling period. Otherwise, the highest waves ranged between 4.2 m and 5.8 m during individual sampling periods.

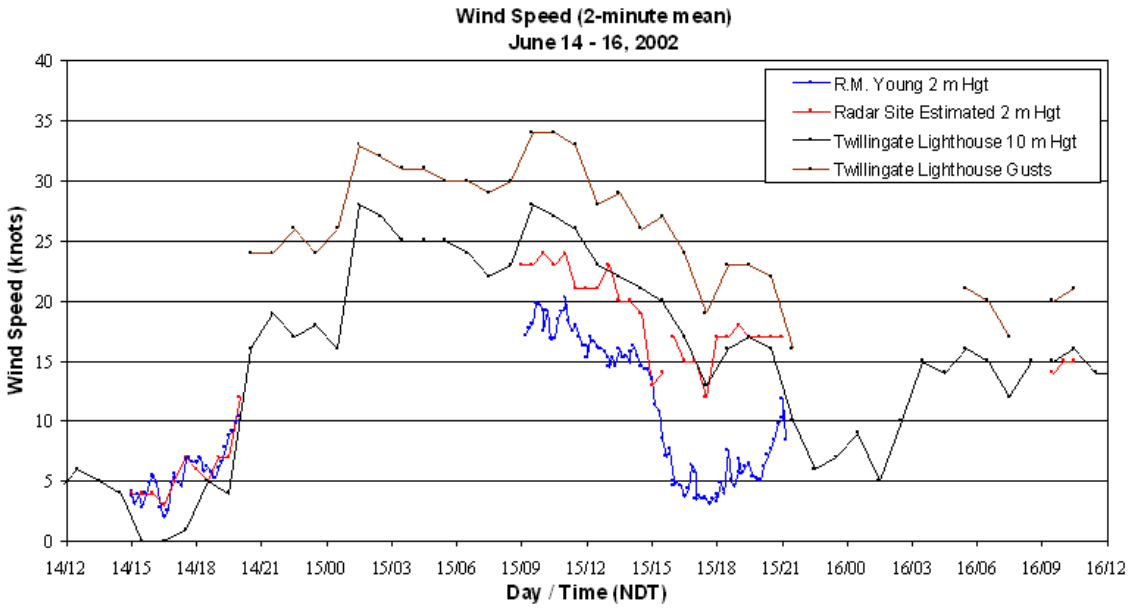


Figure 13. Wind Speed for June 14 to 16

Very poor visibility in fog prevailed early in the day, precluding visual observations of the water surface from the radar site and nearby locations. Consequently, it was not possible to partition the sea state into separate sea and swell components.

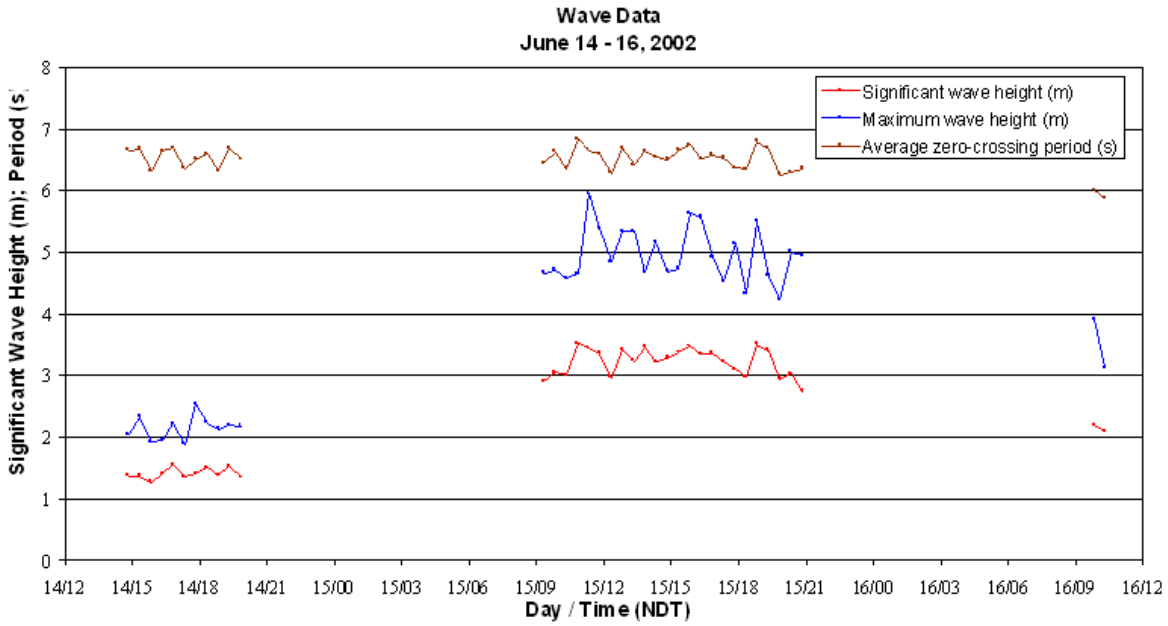


Figure 14. Wave Height for June 14 to 16

However, based on an assessment of the previous observations and the prevailing synoptic weather pattern, it is estimated that the sea state consisted of a northeasterly swell in combination with the northerly wind-sea. About mid-afternoon, the visibility improved sufficiently to visually estimate the sea state. At that point, the wind-sea was estimated to be near 2 m with a characteristic period of near 7 s, while a swell from the north-northeast was estimated to be near 3 m with a period of 10 to 11 s. The wind-sea lowered during the late afternoon to become near 1 m with a period of 4 s by the evening. The swell persisted, however, ranging from 2.8 to 3.3 m with a period near 10 s.

7.4 Iceberg Data

Figures 15 and 16 provide ground truthing pictures of the bergy bit. The iceberg photographs in Figures 15 and 16 were taken with a digital camera. The camera was

Figure 15. Growler and Bergy Bit Targets, 15:46 NDT

calibrated over its zoom range so that accurate target size measurements could be made. Each photograph contains all data on camera settings including focal length and

Figure 16. Growler and Bergy Bit Targets, 15:45 NDT

digital zoom factor, if used. Table 7 presents measurements on the bergy bit. When a review of the photographs was conducted, it was noted that a small piece of ice was located to the west (left of the bergy bit). This target was not observed in the field and no other obvious targets had been detected in the vicinity of the bergy bit during the field trial. The smaller target identified in the photograph was a growler whose size information is presented in Table 7.

Table 7 Iceberg Measurements from Photographs

Date	Time(NDT)	Photo	Length(m)	Height(m)	Description
06/15	15:45:13	4923	6.3	1.8	Bergy Bit 1
06/15	15:45:19	4924	4.5	1.5	Bergy Bit 1
06/15	15:46:17	4925	4.9	1.4	Bergy Bit 1
Average Dimension(m)			5.2	1.6	Bergy Bit 1
Date	Time(NDT)	Photo	Length(m)	Height(m)	Description
06/15	15:45:13	4923	2.5	0.7	Growler 1
06/15	15:45:19	4924	3.2	0.5	Growler 1
06/15	15:46:17	4925	2.5	0.4	Growler 1
Average Dimension(m)			2.7	0.5	Growler 1

7.5 Detection Performance

During the higher sea conditions it was identified that detection did not seem to be as good as the trial that was conducted in 1999 using a 24 RPM antenna. The software had been configured to average up to 64 radar scans. At 24 RPM this equates to 160 seconds of processing time. At 120 RPM 64 scans is only 32 seconds. It was speculated that for the 120 RPM system there was not sufficient time to allow the clutter to fully decorrelate. A modification to the software processing library was made to permit processing up to 256 scans and this version was used for the field trial. This version did provide better detection performance than the 64-scan version. The server PC had 2 GB of main memory and all of this was required for processing of 256 scans of 12-bit radar data.

Figure 17 presents a raw image of the bergy bit and icebergs. It may be seen from the image that there is heavy clutter and even the larger icebergs are not obvious. The medium iceberg at 2 nmi to the north is the iceberg in the background of Figure 10. It is possible to see the shadow from the iceberg in the sea clutter.

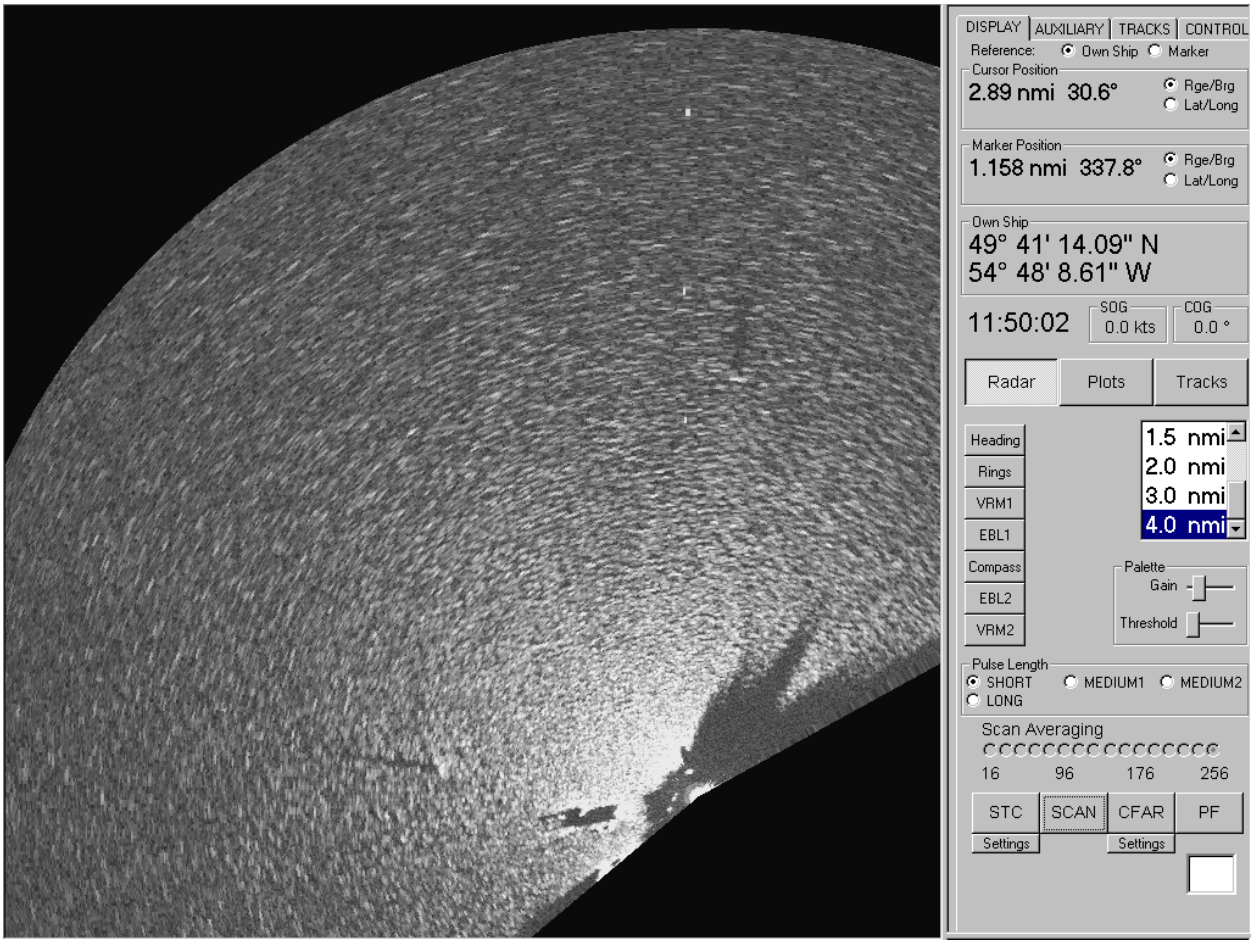


Figure 17. Icebergs in Sea Clutter (Raw Data)

Figure 18 presents the raw data with STC applied to remove some the range dependence in the data.

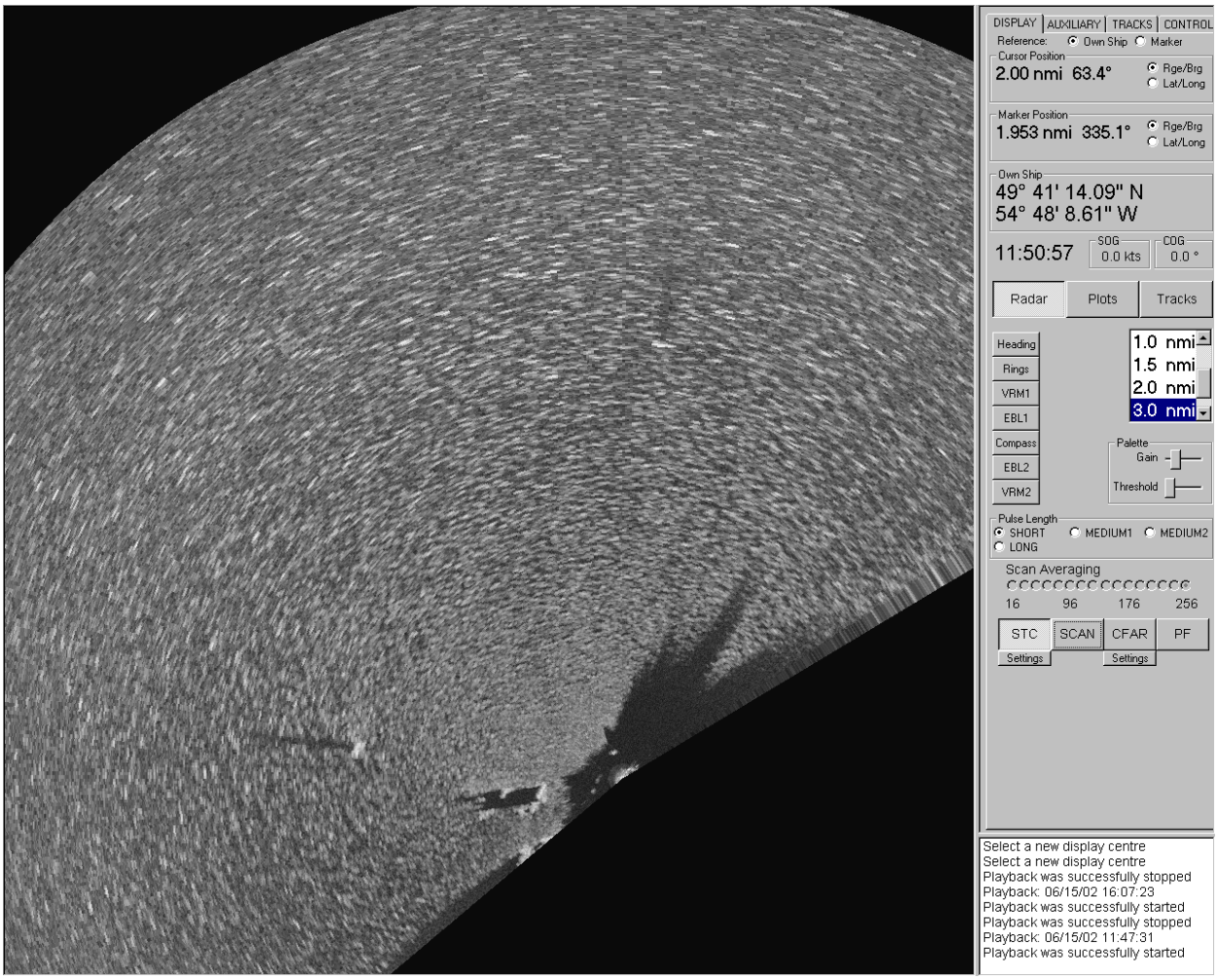


Figure 18. Raw Data with STC Applied

Figure 19 presents results of 256 scans averaged (STC applied). The iceberg to the north and the one to the west become much more obvious. The bergy bit is showing up south of the iceberg to the north.

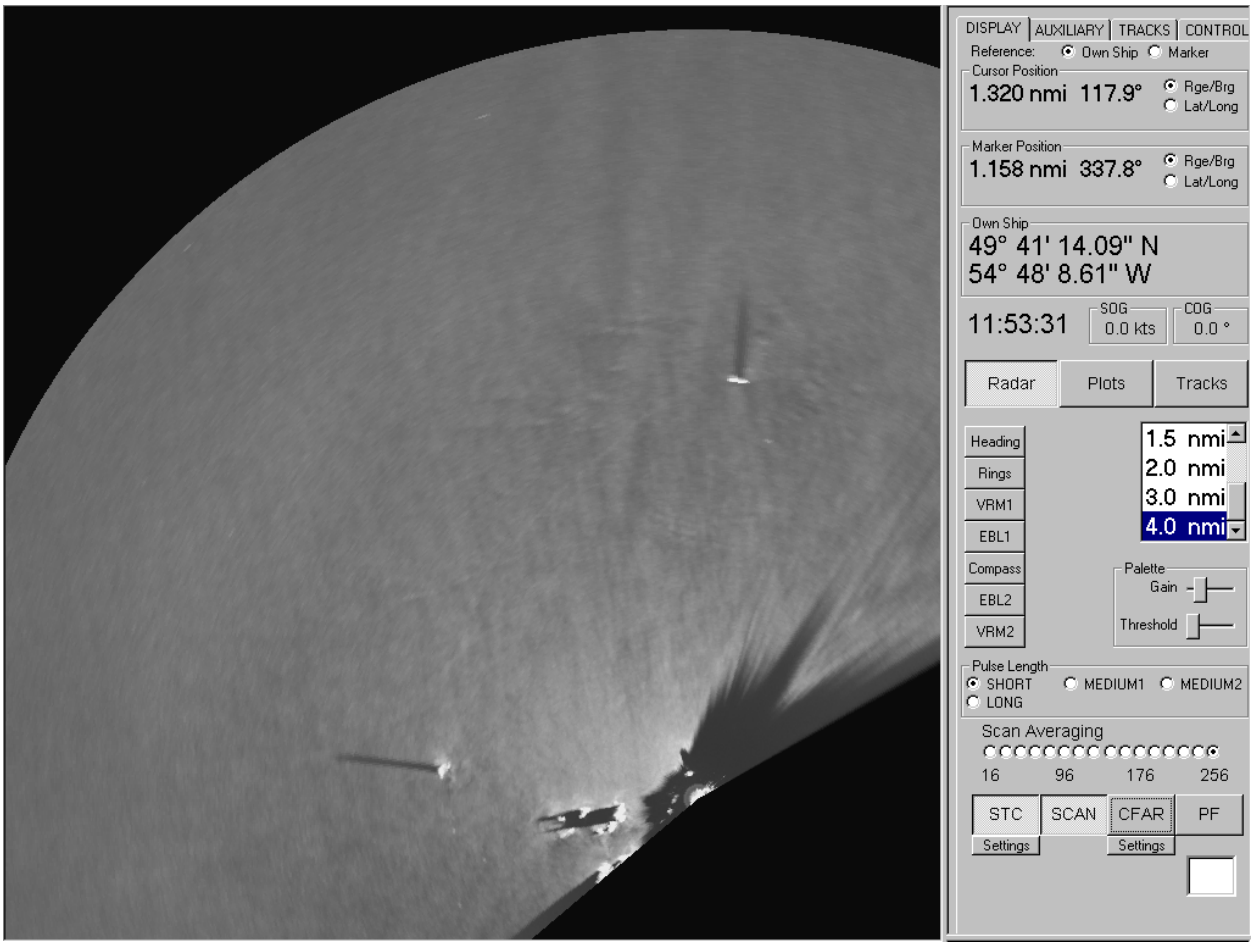


Figure 19. Scan Averaging and STC Applied

Figure 20 provides the results of full processing (STC and 256 scans averaged) with CFAR clutter removal. The bergy bit is now very clearly present.

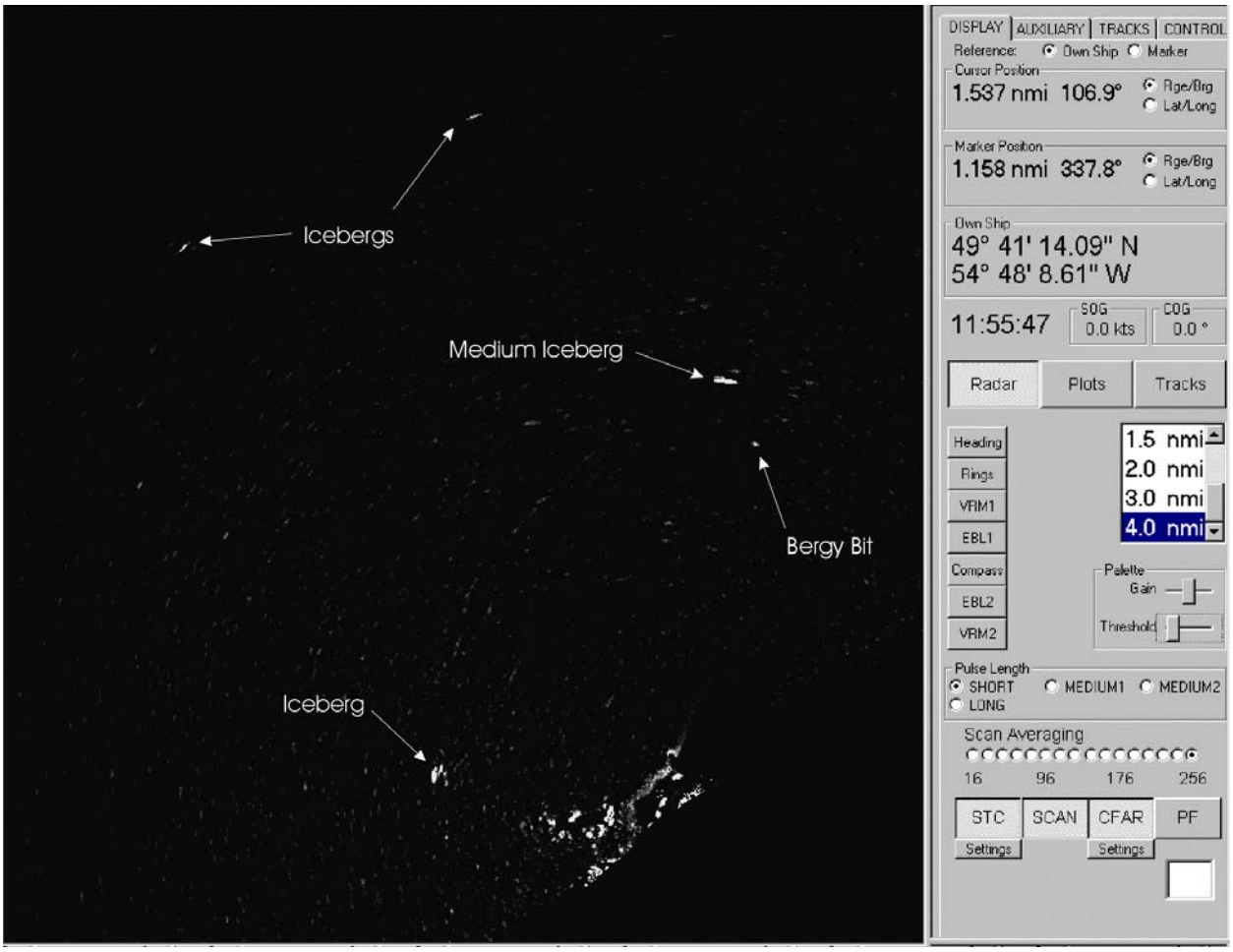


Figure 20. Full Processing Applied

8 CONCLUSIONS

A comprehensive validation program was undertaken to assess the capabilities of the new RSi4000RT radar interface card when used with the SeaScan radar processor. The work was conducted in both laboratory and field settings. The laboratory tests focused on testing the signal-to-noise performance of the new card and testing the system throughput when operating in 12-bit data processing mode. The field testing was used to validate the operational capabilities of the system and to collect a comprehensive data set on icebergs in rough sea conditions.

In order to ready the system for full validation, some redesign work on the existing hardware interfaces was required. This included some minor layout changes to the RSi4000 card to improve noise performance and a redesign of the Composite Video Decoder (CVD). The CVD redesign was required so that it could be used in a PCI slot of the new SeaScan host PC. The measured signal-to-noise performance of the Revision 2 of the RSi4000 was 63 dB with no signal processing and 68 dB with pulse-to-pulse processing applied. This is an excellent result, as the manufacturers' specification for the ADC is 68 dB.

System throughput of the new card, including processing, was measured at 56 MB/s. This far exceeds the requirements of the Raytheon Pathfinder Mk2 at 120 RPM.

Other work was conducted during this project relating to the preparation of the mobile radar unit for field trials and followed by testing the system in an operational role.

A comprehensive field trial was conducted at Twillingate, Newfoundland, in June 2002. During this trial, data was collected on a wide range of iceberg targets from light to heavy sea conditions. The new system demonstrated the ability to provide very good detection capability on bergy bit targets in rough seas. The data collected during the trial will be subject to a follow-on analysis study. During the trial it was identified that it will be necessary to increase the number of scans processed when using the 120 RPM antenna. This should be identified as a task in the data analysis project.

In summary, the tasks undertaken during this project were:

System Characterization

- Repairs to the high-speed scanner: Corrections to electrical wiring and antenna encoding system.
- Production of REV 2 hardware: Corrections to board layout to increase bandwidth and reduce system noise.
- Outfitting of a mobile platform: Modification of a cube van to accommodate radar, related computer equipment and personnel.

Design and Build of the CVD

- Preliminary Design: Submission of a proposal to a consulting firm to procure an implementation of the electrical interface.
- Electrical Interface Review: Cost-benefit analysis of the circuitry proposed, and an assessment of the logic necessary to coordinate the signals and data produced by each interface.
- Logic Synthesis: Design and simulation of the necessary logic in order to prove the feasibility of the design.
- Schematic Design and PCB Layout: Documentation of final electrical interfaces and all required logic; production of PCB Gerber files for fabrication of the board.
- Fabrication: Gerber files and components sent to be manufactured into the prototype board.
- Initial Inspection: Documentation of issues related to board construction. Inspection of the board for proper configuration of power supply. Installation of the board in a PC to verify proper operation of the PCI interface.
- Initial PLD Programming: JTAG interface checked by polling the IDs of the installed PLDs. Testing of separate blocks in stages, where possible, to isolate potential trouble spots.

- Analog Signal Analysis and Final PLD Programming: Final version of all the PLD code sent to the card and any untested analog interfaces fully examined.
- Integration into SeaScan: Integration of the resulting hardware into the mainstream product.
- Preparation for System Characterization: Preparation of production versions of the radar and capture hardware and outfitting of a mobile platform for the project.

System Characterization

- Laboratory Measurements: SNR, platform stability and system throughput measured.
- Field Trials: Field trials conducted in order to fully characterize system performance in comparison to the previous versions.

The RSi4000 radar interface card was thoroughly tested in both the laboratory and its most demanding field application. These tests showed that the interface, when coupled with the Sigma S6 radar processor software, provides very effective real-time detection of small iceberg targets in heavy sea conditions. The analysis showed that for a high-speed scanner it is necessary to process a large number of radar scans to achieve the desired performance.

Appendix A describes the specifications of the final system based on the default configuration of the board as shipped by Sigma Engineering Limited. These specifications offer a range of capabilities and make the RSi4000 suitable for use with most radar systems. Radars having signal specifications outside these may be accommodated by custom factory configuration.

APPENDIX A: SPECIFICATIONS FOR RSI4000-RT-8/12 REV2

SUMMARY OF RSi4000-RT-8/12 FEATURES

The RSi4000-RT-8/12 interfaces to commercial radars with the following specifications:

Radar Trigger

I/O Modes:	single-ended
Absolute Voltage:	-25 V to 25 V
Maximum PRF:	32 kHz
Input Impedance:	75 ohms or High Impedance
Programmable Delay:	up to 4.25 µs in 16.66 ns increments
Hardware Compression:	Optional 2:1

Video

I/O Modes:	single-ended or differential, 8-bit or 12-bit
Absolute Differential Voltage:	-10 V to 10 V
Bandwidth:	60 MHz, limited to 30 MHz with RC filter
Input Impedance:	75 ohms or High Impedance
Sampling Rates (MHz):	60, 40, 30, 20, 10, 7.5, 5 and 2.5
Supported Pulse Lengths:	33 ns minimum
SNR:	63 dB (No processing)
	68 dB (32 pulse processing)

ACP/ARP Configuration

I/O Modes:	single-ended, differential, and RS-422
Input Impedance:	75 ohms or High Impedance
Absolute Differential Voltage:	-5 V to 5 V for 75 ohm 50% duty cycle;
	otherwise -25 V to 25 V.
Required Duration:	22 µs worst case; 4 µs typical

Parallel Angle/CVD Configuration

I/O Modes:	12-bit TTL-level I/O
Handshaking:	Assert 2 µs CB signal during data transition
Connector:	14-pin male ribbon cable mounted on-board

Synchro Configuration

Converter Resolution:	4096 counts = 360 degrees

PCI-bus Interface

Card-to-Card Throughput:	66 MB/s
System Throughput:	56 MB/s (1.6GHz XEON c/w PC800 RAM)
DMA Buffers:	4 to 8 MB allocated from Host RAM
Drivers:	Windows NT, Windows 2000, Windows XP
Diagnostic Utilities:	Error Logging and Sample Capture Utilities
Client/Server Software:	SeaScan server with Seaview client display. Optional tracker software and OEM interface. Raytheon AI tracker support.

APPENDIX B: SIGNAL-TO-NOISE RATIO (SNR) MEASUREMENT THEORY

Signal-to-Noise Ratio (SNR) Measurement Theory

General Description of Analog-to-Digital Converters (ADC)

An analog-to-digital converter (ADC) chip is used to convert an analog signal into a series of digital samples. Theoretically, every sample in the series is separated by exactly the same period in time, and every digital increment corresponds exactly to a constant voltage differential.

To replicate any analog signal perfectly, a perfect ADC would require infinite resolution and infinite sampling rate By the Nyquist criterion, however, it can be shown that a practical ADC can be used to replicate a band-limited signal provided that sampling rates are twice the bandwidth of the signal. In a pristine environment free of all ambient and thermal noise, the practical ADC introduces noise (i.e., less than perfect replication) due to quantization, inaccuracies in the sample clock and linearity of the converter. The signal-to-noise ratio (SNR) is used to measure how close the implementation of the ADC system comes to the theoretical limits. The basic test for measuring the performance of an ADC is simple (in theory): provide a pure sine wave, make sure that the signal exercises the full-scale input range of the ADC without clipping, perform continuous conversions, collect the conversion results, perform a Fourier Transform on the data set and calculate the performance.

Fourier Transform and FFT

One important aspect of the measurement theory is the computation of the Fourier Transform. The Fourier Transform can be a problem for several reasons: a general purpose discrete Fourier Transform algorithm can be computationally demanding and the data set must be “windowed” in order to provide useful results. Rather than use a general purpose discrete Fourier Transform, a specialized form known as the Fast Fourier Transform (FFT) is used. The FFT algorithm requires that the number of conversion results collected from the ADC be a power of 2. In order to produce repeatable AC measurements, larger data sets are used, typically in the range of 1024

to 8192.

The FFT algorithm assumes that the data set represents a repetitive waveform. The two ends of the data must fit together (specifically, the very first data point in the data set must be the same number that would have appeared after the very last data point). The end result is that most manufacturers test with “coherent” input signals. By carefully choosing the input frequency (and/or conversion rate), each data set will be repetitive with the next. For coherent testing, the following mathematical relationship must be met:

Lowest Coherent Frequency = Conversion Rate / Sample Size
Test Frequency = M x Lowest Coherent Frequency (where M is an integer)

The signal generator and the ADC conversion rate must be precise enough to ensure that the input signal is within 1/2 of a least significant bit (LSB) by the end of the data set. This concern is typically addressed by making use of test equipment with sufficient precision to compensate for discrepancies between the oscillators of the signal generator and the ADC. To reduce the concern that coherent testing only tests a small range of the converter’s transfer function, the value of M used for selecting the Test Frequency is always chosen to be an odd number, and ideally should be a prime number.

Ideal SNR

Even in a pristine environment with a perfect ADC, the conversion process from digital to analog introduces quantization noise dependant on the number of bits used to represent the output. The general formula for computing the maximum achievable SNR is:

SNR = 6.02*b + 10.79 + 20*log (A)

where:

b it the number of bits;
A is the normalized RMS gain

The parameter A is typically eliminated by observing the criteria that SNR should exercise the full-scale input range of the ADC without clipping. Without taking this criterion into effect, the value of A is computed from the data using the following formula:

$$A = 0.707 * 1/2 * (Dmax-Dmin+1)/(2^b)$$

Typically, A is set so that Dmax-Dmin is approximately (within 0.5dB of) 2^b-1. This means that the normalized rms value of the gain A is approximately 0.3535 and:

$$SNR = 6.02*b + 10.79 - 9.03 = 6.02*b + 1.76$$

The most widespread use of the ideal SNR is to compute the effective number of bits of the ADC. This is done by solving for b giving a measured SNR. For example, an ideal 12-bit ADC would therefore rate as having a SNR of 74 at all frequencies. In our particular case, the ADC is specified by Analog Devices as having a SNR of 68 dB at frequencies up to 60 MHz. Solving for b indicates that optimal implementation with this ADC will give an effective number of bits of 11.

Parseval's Power Theorem

An essential component of measuring the SNR of the ADC is understanding the Fourier Transform. The Fourier Transform is useful because it provides a model by which to compare the ideal response to measured values. The theoretical basis for doing this is described by Parseval's Power Theorem.

According to Parseval's Power Theorem, the square of the absolute magnitude of the Fourier Transform represents the relative contribution of average power due to each frequency component. For this reason, we refer to the power spectrum as the square of the Fourier Transform. From Parseval's Theorem, a DC level of amplitude V should exhibit a power spectrum component of (V^2)/R at f=0, where R is a system constant representing input resistance. Likewise, a pure sinusoid with a peak-to-peak amplitude

of 2 V would have a total power contribution of ((0.707*V)^2)/R, with half that value at a positive frequency, and half at the negative frequency. To remove the effect of the constant R, it is preferable to use decibels relating the strength of one component to another. It is convenient to measure the signal power relative to a full-scale (amplitude=2 V) DC signal. A sinusoid whose peak to peak value equals the full A/D range would then be defined as having a total average power of 10*log([(0.707*V)^2)/R]/[(2V)^2/R]), or -9 dB. Since half of this would be situated at the negative frequency and half at the positive, each spike would be an additional 3 dB down, making each -12 dB. To compensate for this 12 dB offset, we typically add 12 dB to the computation and speak in terms of dBFS rather than dB. Thus we say that a full-scale DC voltage has a power level of +12 dBFS, while a full scale sinusoid has two power spectrum components of 0 dBFS.

One final note is that if instead of working in the power spectrum we choose to work in the Fourier domain (frequency spectrum), we use Parseval's Theorem to determine that, since Pdbfs=10*log(P)-10*log(Pfs)+12, then

Pdbfs =10*log(FFT^2)-10*log(FFTfs^2)+12
Pdbfs =20*log(FFT) - 20*log((FFTfs) + 12

where

FFT = FFT result corresponding to test frequency
FFTfs=FFT result corresponding to full scale DC signal (computed)

Noise Floor

The noise floor of the Fourier transform is related to the SNR of the ADC. For a simple case, assume that four conversion results are taken from the ADC and processed with the FFT. The result will be two bins: the fundamental and another bin (While the other bin will also be the DC bin, let's ignore that for now.) The SNR of the converter is then distributed between the fundamental and the second bin. So the average noise floor that will be observed in the second bin is 3 dB lower than the converter's SNR.

Likewise, an FFT on eight conversion results will result in a noise floor that is 6 dB lower then the converter's SNR. From this, a general equation can be defined for the noise floor of the FFT:

Noise Floor (in dBFS) = -SNR - 3dB*(log2(N) - 1)

where N is the number of data points used to compute the FFT (1)

Purity of Control Waveform

The final topic in measurement theory is that of signal imperfections in the generation of the waveform. The signal generator used for this test uses a fixed 12-bit, 40 MSPS DAC for generating the desired output waveform. In this mode, spurious signals can be removed using an anti-aliasing filter. To ensure maximum SNR of the generator, certain criteria are outlined in the manual governing amplitude and phase quantization. Specifically, the formulas given for quantization are:

Qa <= -(20*log(N) + 1.8) dBc
Qp <= -20*log(P) dBc

where

N is the number of unique amplitude points in the waveform (up to 4096)
P is the number of points in the waveform

It is generally best to create arbitrary waveforms that use all available data (16,000 points and the full range of DAC codes 0 to 4095). Since it is desirable to match the signal to powers of 2 for FFT purposes, it is necessary to limit the data points to 8192. The resulting phase quantization equates to -80 dBc. Due to symmetry in the sinusoid waveform, less than 4096 unique points will be present in the waveform. The use of prime numbers for the number of cycles included within the 8192 data points helps to maximize this value. Optimal results were found to occur when 3 cycles over 8192 samples were selected, yielding 4095 unique data points. The resulting amplitude quantization is -70 dBc. The natural sampling rate (without interpolation by the

generator) is 14,648.4375 Hz.

Finally, the video output of the signal generator is designed ideally for differential video. Consequently, the RSi4000RT should be operated in differential video mode in order to ensure that the highest level of SNR is available from the analog video source.

Frequency Spectrum of an Ideal ADC

Based on the preceding analysis, the frequency spectrum of an ideal 12-bit ADC was computed from 4096 samples based on a 20 MHz sampling rate and a test frequency of 14.6484375 kHz (3 cycles). The expected result should have two 0 dBFS spikes corresponding to the positive and negative frequency components, and a noise floor of (-74 - 3*(log2(1024)-1) = -101 dBFS. A spreadsheet was created in Microsoft Excel using 32-bit calculations which were converted to 12-bit resolution at the final step. The resulting power spectrum is shown in Figure B-1.

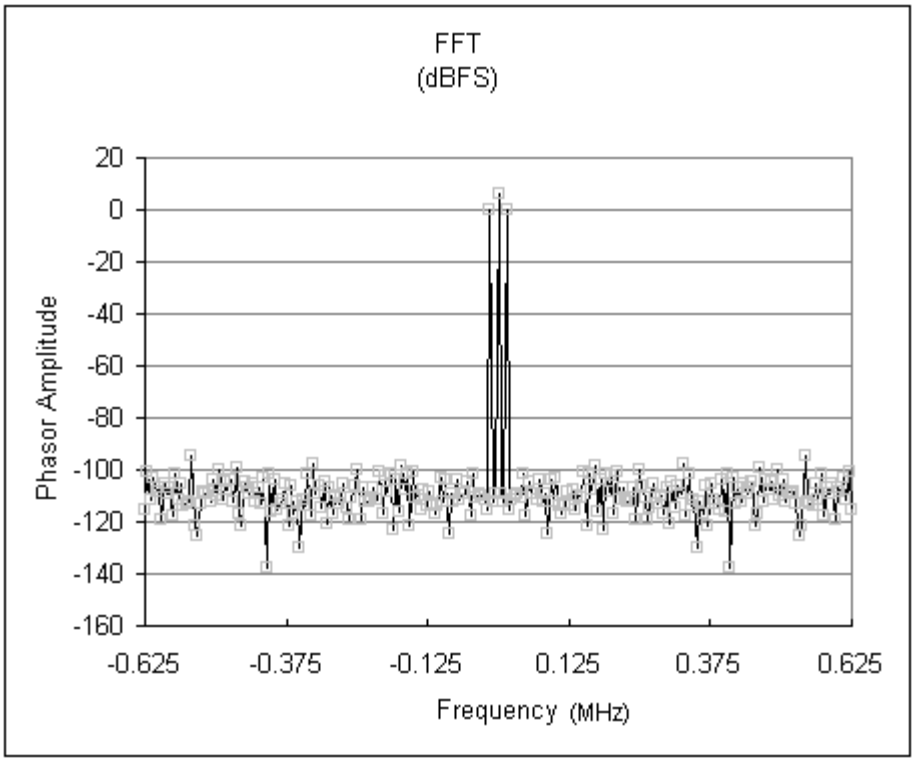


Figure B-1. Power Spectrum of an Ideal ADC

As a final check of the accuracy of the implementation, the SNR was computed by summing the squares of the FFT phasor amplitudes corresponding to signal/harmonic components (not including the DC component). All non-signal components were similarly tallied (except for the DC component). The ratio of the signal to non-signal components was then computed and was found to be 74.78 dB.

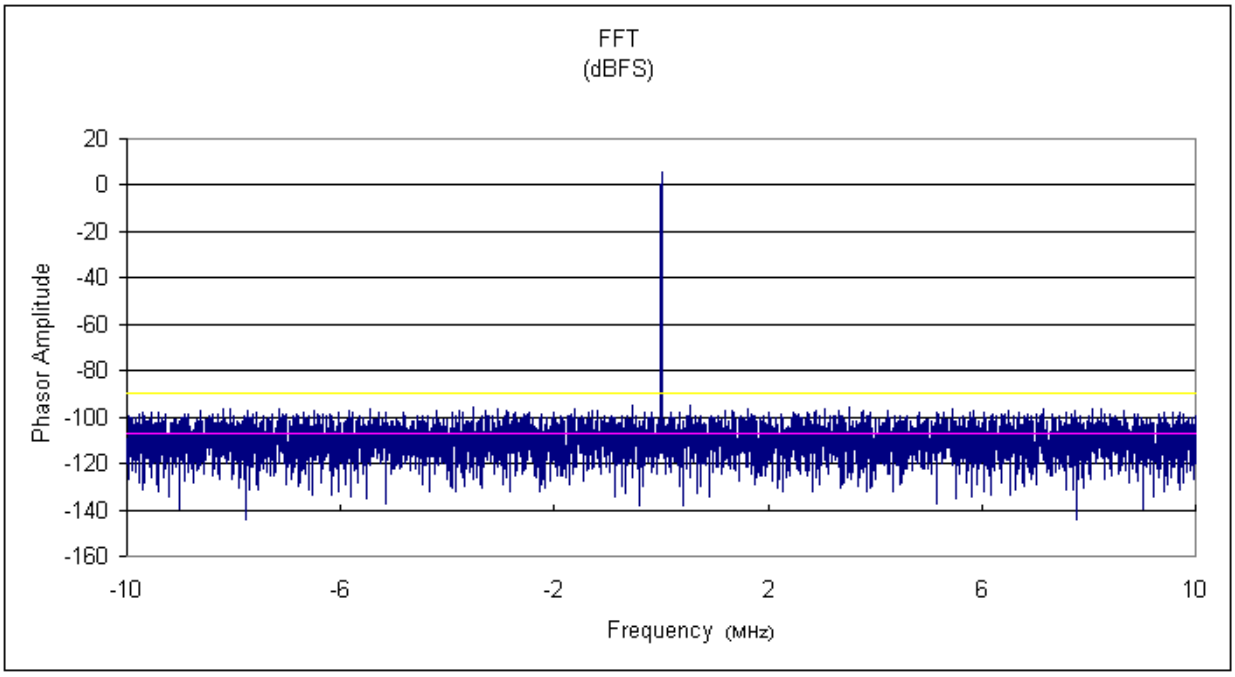
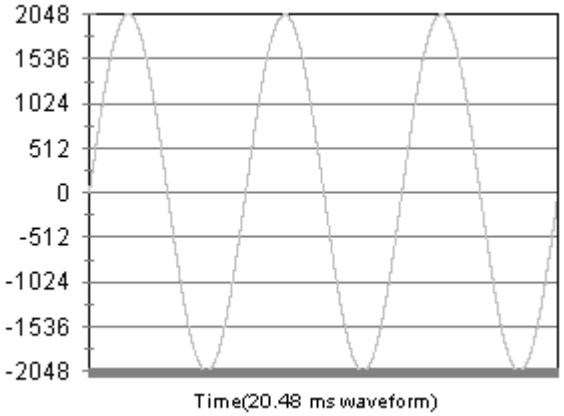


Figure B-2. Power Spectrum of Simulation for 10 MHz Bandwidth

APPENDIX C: RS232 INTERFACE SOFTWARE FOR THE HP33120A

RS232 Interface Software for the HP33120A

A QBASIC program named BASOUT.BAS was used to download arbitrary waveforms to the arbitrary waveform generator. ALIGN4.TXT, the actual file used for testing, contained 8192 12-bit samples defining 3 cycles of a sinewave. The “natural frequency” of the test pattern at 40 MSPS is given as ((40MHz/8192)*1000) = 4.8828125 kHz.



```
INPUT "ENTER A FILE NAME:", a$
REM OPEN "COM2:4800,n,8,1,LF,CD0,CS0,DS0,OP0,RS,TB2048,RB2048" FOR OUTPUT AS #1
OPEN "com2:4800,o,7,2,LF,CD,RS" FOR OUTPUT AS #1 LEN = 1000
OPEN a$ FOR INPUT AS #2
j = 0
WHILE NOT EOF(2)
      LINE INPUT #2, i$
      IF (RIGHT$(i$, 1) = ",") THEN
            PRINT #1, i$;
      ELSE
            PRINT #1, i$
      END IF
      IF ((INT(j / 100) = j / 100)) THEN PRINT ".";
      j = j + 1
WEND
CLOSE 1
CLOSE 2
SYSTEM
```

BASOUT.BAS

APPENDIX D: RAYTHEON CANADA MHT UPGRADE FINAL REPORT

Raytheon

Search and Rescue Tracker

Modifications for 12-Bit Sea Scan

Prepared for:

Sigma Engineering for
Transportation Development Centre
Transport Canada

by:

Raytheon Canada Limited
June 2002

1 Overview

The Search and Rescue Tracker presently uses the Sigma Engineering Sea Scan software running on a PC with a proprietary 8-bit radar acquisition card to process the radar video signal into detections. These detections are then correlated into high confidence tracks by two or more additional PCs.

Sigma Engineering have developed a 12-bit radar acquisition card to improve performance. The purpose of this contract was to modify the SAR Tracker to work with the new card and its associated software. Limited functional testing was done with recorded data from St. John's harbour and from the rooftop radar installation in Waterloo.

2 Changes to SAR Tracker

After performing a system-wide code review of the full HCTracker software, we determined that the changes required to support Release 4.2 of the SeaScan software package would be localized within two functional areas, the ATC (Automatic Threshold Control) and MofNAnal (M of N analytical pre-filter) tasks. The ATC takes raw data from the SeaScan and feeds back threshold maps, and MofNAnal pre-filters incoming samples, and passes them on to the MHTracker in a format which is not affected by the changes in data. Similarly, all functional components which are downstream of the MHTracker are not affected by the change, because the data components they draw from the SeaScan do not include raw sample data.

The HCTracker is written in a mix of C/C++ so whenever we integrate with a new release of the Sigma software, we rearrange the structure of the header files to simplify their incorporation into our system. This procedure proceeded without problems, and the new versions of the header files produced no unexpected surprises.

We considered the option of modifying the system so that it could run in either 8-bit or 12-bit sampling mode, as specified by a configuration parameter, but decided that this unnecessarily left us open to end-user problems via improper configuration settings. The amount of extra code required to "bullet-proof" us against these was not considered worthwhile, given that we can see no reason for field systems to switch between 8-bit and 12-bit sampling during normal operation. Therefore, we decided to base the 12/8-bit decision on a #define statement in the global header, which would allow us to build releases of the system which support one mode or the other.

Field testing the new card in 8- and 12-bit mode will require building two releases and starting the appropriate executable.

The ATC and MofNAnal code was then examined and modified as required, so that all data components which depend on sample size are controlled by this global definition. When these changes had been implemented and unit tested, two versions of the system (8- and 12-bit) were built and prepared for testing.

3 Test Results

The initial test of the rebuilt system (12-bit version) proved inoperable. Although we had made no hardware or network modifications from the previously running test system, neither the HCTracker nor the Sigma-supplied sample client application were able to draw samples from the newly installed version of the SeaScan software. After some interaction with Sigma and a variety of elimination tests, we determined that there was a problem with the supplied version of the client.dll. This was replaced by Sigma, and we proceeded with the modified test version of Release 4.2.

Once this was in place, tests proceeded with the version of the SeaScan server provided, which uses one of the two disk-based data files, containing short and medium pulse samples, in place of live data.

Multi-hour (overnight) tests were run with each of the (short/medium) test files. There

were no observable problems or failures with either file.
The system found and displayed tracks normally. From visual observation of the radar data, these tracks appeared to represent real targets. The system is not located where any testing with marine targets is possible.

Image masks and threshold maps were sent successfully to the new version of the software, and it responded appropriately.

The main observed difference between this version of the Sigma product and the previous version is that Release 4.2 functioned more slowly, requiring 3-4 additional seconds per iteration for data to pass through the MofN pre-filter to the MHTracker. Upon later tests with a live radar, we observed that this speed differential diminished, suggesting that a substantial portion of the slowdown was due to the amount of simulated data being pulled off the hard drive rather than the near-doubling of the amount of data being transferred across the network.

A 12-bit radar digitization card was then added to the system, and the Sigma test software replaced by the SeaScan V4.2, Build 1 release kit. The digitization card was mounted in the Advantech chassis which is the standard HCT hardware configuration.

Multi-hour (overnight) tests were run with the HCT software built in each of the 12/8-bit configurations. The SeaScan/SeaView software was run continuously throughout all tests, rather than being stopped and restarted when we changed the HCT software build from 12- to 8-bit.

No operational differences were observed between the new 8-bit configuration and the previous release of the Sigma package. In the 12-bit configuration, a slight decrease to the update rate was observed due to the increased amount of data being transferred among system components. This update rate, however, remained within acceptable limits. During the system testing we experienced very infrequent system crashes on the primary Tracker but we were already tracking this problem in the HCT software and therefore believe it has nothing to do with the installation of the new Sigma package.

4 Conclusions

SeaScan V4.2, Build 1 and the associated 12-bit digitization card are compatible with the HCT configuration.

The digitization card is compatible with the Advantech chassis, and caused no lock-ups or other observable hardware malfunctions within the time period of these tests.