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Shuttle Tanker Radar Detection Trials and RSi4000-RT-8/12 Development

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by
J. Ryan, S. Motty, M. Johnson
Sigma Engineering Limited

March 2003

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16. Abstract

The Shuttle Tanker Radar Detection Trials were conducted in the spring of 2000. The objective of the trials was to investigate the operational iceberg detection capability of the advanced MRI (Modular Radar Interface) with the high-speed (120 rpm) radar scanner. The equipment was successfully installed and put into service; however, it turned out to be a light ice year and no icebergs were encountered during the trials. The equipment was left for the crew of the tanker *M.T. Kometik* to use until October 2000 and was then removed.

During the second phase of the project, Sigma Engineering Limited undertook the development of a 12-bit PCI-based A/D card (known as the RSi4000-RT-8/12) for enhancement of radar video. The card simplifies the hardware of the previous generation of interfaces by offloading some functions to the host CPU.

Because of the checks and balances inherent in the design methodology, problems encountered in the first build of the RSi4000-RT-8/12 were minimal. With the system components fully debugged, the card was integrated into the MRI software previously developed by Sigma Engineering Limited in conjunction with the Transportation Development Centre. Throughputs up to 24 MB/s were realized on a development platform consisting of a Pentium 2 motherboard with a 350 MHz processor. Later testing on Pentium 4 platforms gave data capture rates up to 56 MB/s. These results make previously demanding radar applications easily achievable with the new MRI.

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16. Résumé

Les essais de détection radar à bord du pétrolier navette ont été effectués au printemps 2000. Ces essais avaient pour objectif d'étudier la capacité opérationnelle de détection d'icebergs par l'interface modulaire radar (IMR) avancée couplée à l'antenne radar à haute vitesse (120 tr/min). L'équipement été installé et mis en service avec succès. Or, comme il y a eu peu de glaces cette année, aucun iceberg n'a été rencontré durant les essais. Le matériel a été laissé en service à bord du pétrolier *M.T. Kometik* jusqu'au mois d'octobre 2000, puis retiré du navire.

Durant la deuxième phase du projet, Sigma Engineering Limited a entrepris la mise au point d'une carte A/N PCI 12 bits (désignée RSi4000-RT-8/12) destinée à améliorer le signal vidéo du radar. Cette carte décharge l'unité centrale de traitement de certaines fonctions, simplifiant ainsi le matériel de la génération précédente d'interfaces.

En raison des autocontrôles intégrés, les problèmes de la première version de la carte RSi4000-RT-8/12 étaient minimes. Les composants du système étant au point, il a été possible d'intégrer la carte au logiciel IMR préalablement développé conjointement par Sigma Engineering Limited et par le Centre de développement des transports. Des débits de traitement jusqu'à 24 Mb/s ont été réalisés sur une plate-forme de développement consistant en une carte-mère Pentium 2 avec processeur de 350 MHz. Des essais sur plates-formes Pentium 4 ont donné des débits de 56 Mb/s. Compte tenu de ces résultats, les applications radar autrefois exigeantes sont désormais faciles à exploiter avec la nouvelle interface IMR.

17. Mots clés	18. Diffusion
Détection d'icebergs, interface modulaire radar, IMR, antenne radar à haute vitesse, RSi4000-RT-8/12, carte d'interface radar, amélioration du signal vidéo	Le Centre de développement des transports dispose d'un nombre limité d'exemplaires.

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EXECUTIVE SUMMARY

The Shuttle Tanker Radar Detection Trials were conducted in the spring of 2000 onboard the *M.T. Kometik*. The *Kometik* transports oil from the Hibernia oil production platform to either the transshipment facility in Newfoundland or directly to market on the east coast of Canada or the United States. The vessel is 272 m long and has a gross tonnage of 76,000. The route of the *Kometik* can result in encounters with icebergs. The objective of the trials was to investigate the operational iceberg detection capability of the advanced MRI (Modular Radar Interface) with the high-speed (120 rpm) radar scanner. The intention was to expose tanker operators to the latest iceberg detection technology and to collect data on smaller iceberg sizes, including bergy bits and growlers.

The equipment was successfully installed and put into service; however, it turned out to be a light ice year and no icebergs were encountered during the trials. The equipment was left for the crew to use until October 2000 and was then removed. No iceberg data was collected so the data analysis task of the project was not required.

During the second phase of the project, Sigma Engineering Limited undertook the development of a new radar interface card. This card was designed to overcome many of the shortcomings of the radar interface hardware used with the MRI and provide 12-bit high dynamic radar video data for improved detection performance. The new card is a 12-bit PCI-based A/D card (known as the RSi4000-RT-8/12) for enhancement of radar video. The card takes advantage of previous generation interfaces and simplifies much of the hardware by moving some hardware functions to the PC.

The approach used in the design was based on past success in hardware design and fabrication. A preliminary design was delivered to a consulting firm in order to produce an electrical interface design. Onboard logic for control of the electrical interface was then developed and prototyped. The logic established the theory of operation of the board, making it possible to develop a device driver for testing the prototype. With the driver and prototype working, a sound basis was available for deciding whether to proceed with the first build of the design.

Because of the checks and balances inherent in the design methodology, the first build of the RSi4000-RT-8/12 has been a complete success. Most problems were of a mechanical nature related to sizing and placement of the components on the board. These problems can be easily corrected in subsequent builds, but do not affect the usability of the first generation of cards in the intended application.

Very few problems of an electrical nature were found in the fabricated boards. The most significant of these related to the circuit used for ACP and ARP detection. This problem was corrected by installing pull-up resistors on the output side of the opto-couplers used in the ACP and ARP interface.

The only other modification of significance between the prototype and the first generation board relates to the use of memory in the device driver. Originally, a special type of memory shared by the application, driver and hardware had been used. It was found that application-level access to this memory carried a heavy performance penalty. Consequently, a call was added to the driver so that the application could pass it the address of a conventional buffer. The driver could then perform the copy efficiently on behalf of the application. The size of the internal buffers was found to affect system throughput, with 2 MB buffers allowing throughputs up to 16 MB/s, and 4 MB buffers allowing throughputs up to 24 MB/s. These results were obtained on a development platform consisting of a Pentium 2 motherboard with a 350 MHz processor. Later testing on Pentium 4 platforms gave data capture rates up to 56 MB/s.

With the system components fully debugged, the card was integrated into the MRI software previously developed by Sigma Engineering Limited in conjunction with the Transportation Development Centre.

SOMMAIRE

Les essais de détection radar à bord du pétrolier navette *M.T. Kometik* ont été effectués au printemps 2000. Le navire transporte du pétrole de la plate-forme de production Hibernia vers l'installation de transbordement de Terre-Neuve ou directement vers les marchés de la côte est du Canada et des États-Unis. Il s'agit d'un pétrolier de 272 m de longueur ayant une jauge brute de 76 000 tonnes. Des icebergs se trouvent parfois sur la route du *Kometik*. Les essais en mer avaient pour objectif d'étudier la capacité opérationnelle de détection d'icebergs par l'interface modulaire radar (IMR) avancée couplée à l'antenne radar à haute vitesse (120 tr/min). Il s'agissait de mettre les opérateurs du pétrolier en contact avec la dernière technologie de détection des icebergs et d'acquérir des données sur les petits icebergs, y compris les bergy bits et les bourguignons.

L'installation et la mise en service de l'équipement ont été couronnées de succès. Or, comme il y a eu peu de glaces cette année, le navire n'a rencontré aucun iceberg durant les essais. Le matériel a été laissé à bord du navire, en service, jusqu'au mois d'octobre 2000, après quoi il en a été retiré. Les chercheurs n'ayant pu recueillir de données sur les icebergs, il n'y a eu aucune analyse.

Durant la deuxième phase du projet, Sigma Engineering Limited a entrepris la mise au point d'une nouvelle carte d'interface radar, conçue pour pallier un bon nombre de lacunes du matériel d'interface utilisé avec l'IMR et pour fournir un traitement 12 bits à dynamique élevée du signal vidéo de radar, pour une détection plus performante. Il s'agit d'une carte A/N PCI 12 bits (désignée RSi4000-RT-8/12), destinée à améliorer le signal vidéo du radar. La carte utilise des interfaces de la génération précédente et simplifie une bonne partie du matériel en confiant certaines fonctions au micro ordinateur.

La méthode de conception était fondée sur l'expérience antérieure d'étude et de fabrication de matériel. Une étude d'avant-projet sommaire a été remise à une firme de consultants avec le mandat de produire une interface électrique. On a ensuite développé et prototypé une logique de commande embarquée de l'interface électrique. La logique établissait le principe de fonctionnement de la carte, ce qui a permis de mettre au point un pilote de périphérique pour l'essai du prototype. Le pilote et le prototype étant opérationnels, on disposait alors d'une base solide pour décider ou non de réaliser la première version du concept.

Grâce aux autocontrôles intégrés, la première version de la carte RSi4000-RT-8/12 s'est révélée un succès complet. Les problèmes rencontrés étaient pour la plupart de nature mécanique et concernaient le dimensionnement des composants et leur positionnement sur la carte. Ces problèmes pourront être facilement corrigés sur les cartes subséquentes et ne nuiront pas non plus à l'utilisation de la première version aux fins prévues.

Les cartes fabriquées ont démontré très peu de problèmes électriques, les plus importants étant reliés au circuit de détection ACP et ARP. La correction a consisté à installer des résistances de polarisation à l'alimentation sur la sortie des opto-couplers utilisés dans l'interface ACP et ARP.

La seule autre modification importante entre le prototype et la première génération est reliée à l'utilisation d'une mémoire dans le pilote de périphérique. Au début, une mémoire spéciale était partagée par l'application, le pilote et le matériel. Il a été constaté que l'accès à la mémoire par l'application entravait énormément la performance; un appel a donc été ajouté au pilote pour que l'application puisse passer avec l'appel l'adresse d'une mémoire tampon classique. Le pilote pouvait ensuite copier les données de manière efficace pour le compte de l'application. On a découvert que la capacité de la mémoire tampon interne influait sur le débit de transmission du système, qui pouvait atteindre jusqu'à 16 MB/s avec des tampons de 2 MB, et jusqu'à 24 MB/s avec des tampons de 4 MB. Ces résultats ont été possibles sur une plate-forme de développement constituée d'une carte-mère Pentium 2 avec processeur de 350 MHz. Des essais ultérieurs sur plates-formes Pentium 4 ont produit des saisies de données jusqu'à concurrence de 56 MB/s.

Une fois les composants au point, la carte a été intégrée au logiciel IMR qui avait été développé par Sigma Engineering Limited conjointement avec le Centre de développement des transport.

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GLOSSARY OF ACRONYMS

A/D	Analog-to-Digital
ACP	Azimuth Count Pulse
ADCLK	Analog-to-digital Clock
AI	Artificial Intelligence
ARP	Azimuth Reset Pulse
CAPB	Capacitor Bottom
CAPT	Capacitor Top
CCG	Canadian Coast Guard
CPLD	Complex PLD
CVD	Composite Video Decoder
DAC	Digital to Analog Converter
DLL	Dynamic Link Library
DMA	Direct Memory Accress
(E)EPROM	(Electrically) Erasable PROM
FIFO	First In, First Out memory
GND	Ground (0 V)
GPS	Global Positioning System
IRQ	Interrupt Request Level
LED	Light Emitting Diode
MHT	Multiple Hypothesis Tracker
MRI	Modular Radar Interface
MSPS	Million Samples Per Second
OLS	Offshore Loading System
PC	Personal Computer
PCB	Printed Circuit Board
PLCC	Plastic Leaded Chip Carrier
PLD	Programmable Logic Device
PRF	Pulse Repetition Frequency
PROM	Programmable Read-only Memory
RAM	Random Access Memory
RSi	Radar Signal Interface (Input)
TTL	Transistor-Transistor Logic

1. INTRODUCTION

The Transportation Development Centre (TDC) is involved in a variety of projects aimed at developing techniques and systems to enhance the small target detection capability of radar for use in Search and Rescue and iceberg detection.

The MRI (Modular Radar Interface) was developed over a number of years, first using the TITAN radar processor as the prime radar interface and subsequently using the RSi3000/PDI card set for that purpose. The current version of the MRI was used successfully in field trials for Search and Rescue in 1997 onboard the Coast Guard vessel *Bernier*. During those trials a large amount of raw radar data was collected to evaluate the AI Tracker developed by Raytheon Canada. The trials and subsequent report (TP 13236E) identified a number of problems with the MRI and high-speed scanner.

The scope of work identified for the Shuttle Tanker field trials was primarily to gain operational experience using the MRI with the AI Tracker in the role of iceberg detection. The target platform for the technology was the shuttle tanker used for transporting oil from oil production platforms off the coast of Newfoundland to port. A review of available platforms was conducted and it was decided that, for the best operational data, the most suitable platform was the shuttle tanker *Kometik*. The *Kometik* transports oil from the Hibernia oil production platform to either the transshipment facility in Newfoundland or directly to market on the east coast of Canada or the United States. The vessel is 272 m long and has a gross tonnage of 76,000. The route of the *Kometik* can result in encounters with icebergs. The objective of the trials was to investigate the operational iceberg detection capability of the advanced MRI (Modular Radar Interface) with the high-speed (120 rpm) radar scanner. The intention was to expose tanker operators to the latest iceberg detection technology and to collect data on the smaller iceberg sizes, including bergy bits and growlers.

In the winter of 2000 repairs were undertaken to remedy the azimuth wobble problem in the high-speed scanner identified in the 1997 field trials on the *Bernier*. These repairs resulted in a significant reduction in the amount of azimuth shifting in the radar data from scan to scan; however, it was not completely eliminated. A summary report of the repairs in provided in Appendix D.

The complete MRI system was successfully installed and put into service; however, it turned out to be a light ice year and no icebergs were encountered during the trials. The equipment was left for the crew to use until October 2000 and was then removed. No iceberg data was collected so the data analysis task of the project was not required. Section 2.1 provides a summary of the *Kometik* trials and presents some sample data from the MRI.

In the second phase of the project, Sigma Engineering Limited undertook the development of the next generation radar interface card. The objective of the development was to eliminate all of the shortcomings of the present MRI interface technology and to provide superior signal fidelity for improved target detection performance.

Sigma Engineering Limited has developed a number of commercial products that enhance radar images through the use of high-speed scanners and high-definition digital acquisition. In the second phase of the project the company produced a new generation of radar capture cards that combine the high bandwidth of the PCI Interface with the high-definition of a 12-bit A/D chip. The resulting product is marketed under the name of RSi4000-RT-8/12.

The RSi4000-RT-8/12 product is the result of more than 10 years' experience in the field of radar capture. It combines all the interface circuitry required to digitize images from most commercial radar in a single PCI-bus card. This document is the final report describing the design and implementation of the 12-bit radar capture card for the PCI bus. Some software was also included in the development by drawing upon existing intellectual property. This software includes a device driver for Windows NT and Windows 2000, and an installable diagnostic service with help files.

2. BACKGROUND

Radar capture products allow images from a live radar to be viewed in real time on a personal computer (PC). The computer images are in digital form, and can be processed and enhanced by software under control of the computer operator. This feature significantly improves the ability to use radar for detection of nearby and distant objects in all weather conditions.

With over 10 years' experience in the development of software for enhanced radar detection, Sigma Engineering Limited has relied upon many radar capture products, most recently the BarcoView RS1000 Radar capture card, which it supports under the model name RSi4000A. This card, like all past endeavours undertaken by the company, is restricted to 8-bit digital video.

Technology has now advanced to the point where processing techniques can make use of higher resolution video to improve the signal-to-noise ratio of radar even further than in the past. To do so, it was resolved to develop a straightforward, radar-specific capture card with support for up to 12 bits of digital resolution.

2.1 Trials on the *Kometik*

It was desired to evaluate the performance of the pre-existing SeaScan radar processor in an operational scenario, using a high-speed scanner. Sigma uses the trade name SeaScan for the MRI (Modular Radar Interface). The targets of interest were icebergs, bergy bits and pack ice. Where possible, it was desired to collect data on these targets. The tracking performance of the Raytheon Canada Multiple Hypothesis Tracker (MHT) was also to be evaluated. The SeaScan server was modified to support some additional features that would improve the performance of the Raytheon MHT.

From May 2 to 4, 2000, a complete SeaScan system was installed on the *Kometik*, one of the shuttle tankers used in the Hibernia oil field. The Raytheon MK2 radar used in previous field trials in 1997 was mounted on the forward mast of the tanker. The scanner of this radar had been modified to run at 120 rpm. The main radar processor was mounted in the electrical room behind the bridge. The system was interfaced to the ship's gyro and GPS devices.

A separate display system was mounted on the bridge and connected to the server via a network link.

Several problems related to powering the radar scanner were encountered during the initial installation. The scanner motor was drawing too much power during startup from the standard ship supply. When the power source was changed, the scanner would

start but soon quit due to overheating. It was decided to replace the motor with a more powerful one.

On May 11, 2000, the new motor was installed and the radar installation was finished. The hard disk in the display PC failed, resulting in the delay of the first voyage.

Installation was completed on May 16, 2000. The first field trial began the following day in Placentia Bay. The *Kometik* picked up a load of oil from the Hibernia platform and delivered it to Philadelphia. Four tapes of data were collected on the voyage out to Hibernia, two tapes were collected while oil was being loaded, and four tapes were collected on the trip to Philadelphia.

Near the end of the voyage, it was noticed that the scanner was not rotating as fast as normal (120 rpm). When the ship returned to Newfoundland, the system was checked and found to have a loose drive belt. At the same time, a full system check was performed and it was noticed that the video levels were considerably degraded. Discussions with the manufacturer concluded that some components needed to be replaced. Arrangements were made to send the components to Halifax for installation when the *Kometik* next made port.

On June 12, 2000, representatives from Sigma and Raytheon Canada met in Halifax to install the MHT while the radar was being repaired. The intention was to perform another sea trial, collecting data and training the crew on the use of the MHT. However, the wrong components had been supplied for the radar, and the repair could not be completed. The sea trial was therefore cancelled.

On June 21, 2000 another visit was made to the ship in Halifax. The technicians completed the installation of the replacement components, but the radar still performed poorly. Video levels were extremely low and the system was not usable. The sea trail was again cancelled. The ship was due to visit Portland, where a representative from Raytheon would board the ship to check the system. This visit was successful in restoring full system functionality.

However, by this time, the ice season offshore Newfoundland was over. It had been an extremely light ice season, and it was felt that no further opportunities for ice encounters would arise. The SeaScan system was left onboard for evaluation by the ship's crew. However, the Raytheon MHT system was never put into operation.

The system was removed from the *Kometik* over two visits (October 17 and 23, 2000). Overall, the crew of the *Kometik* was impressed by the system, and had several suggestions regarding features they felt were important to make the system more functional.

Figures 1 and 2 are examples of the data collected during the sea trail. This data is taken from Placentia Bay, just north of Argentia. Figure 1 shows the raw data and Figure 2 has full processing applied (32 scans averaged). The small targets to the east and south of the vessel are markers for fishing gear, typically small plastic floats. Occasionally some of the markers have an extra radar reflector attached.

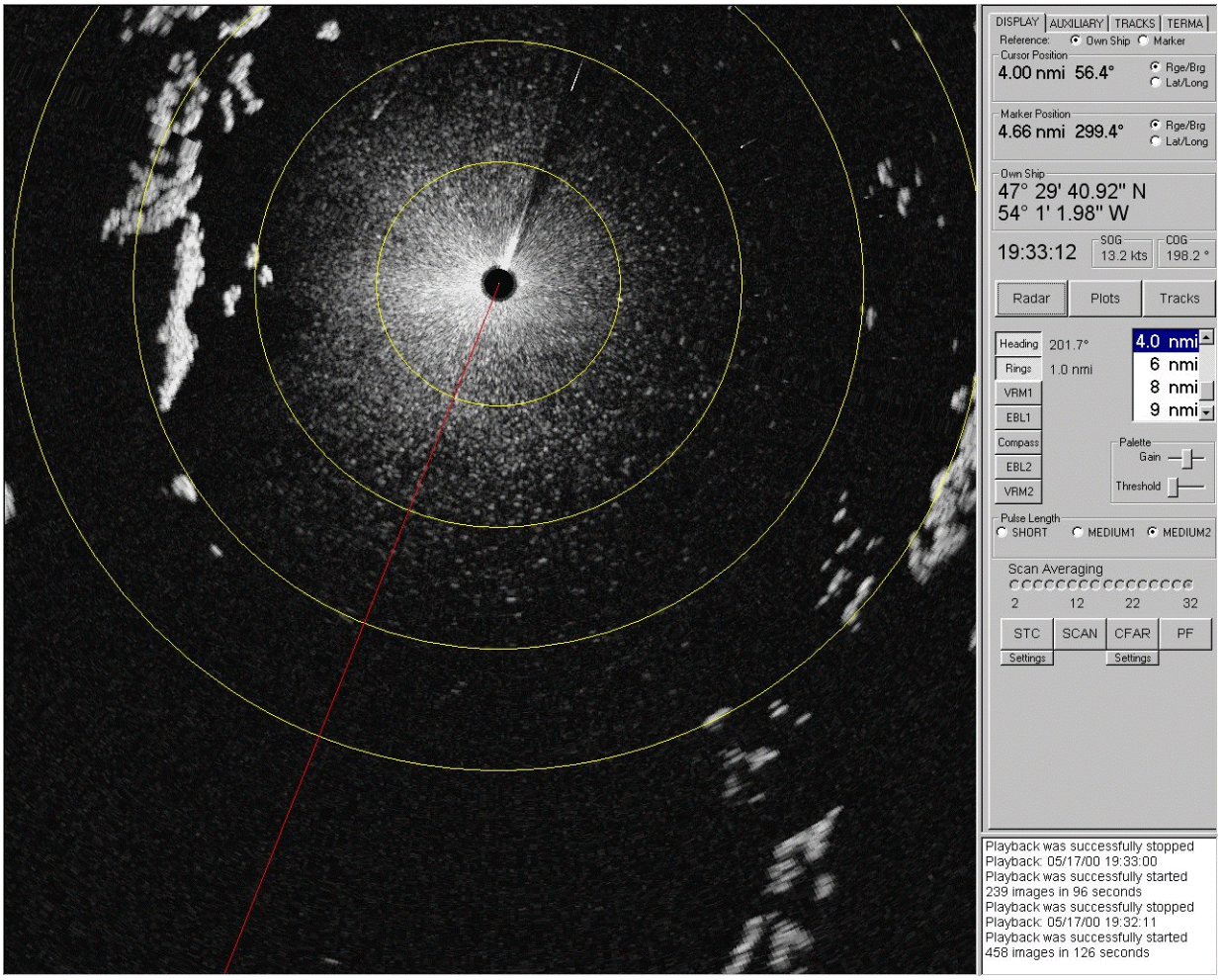

Figure 1: Placentia Bay (unprocessed radar image)

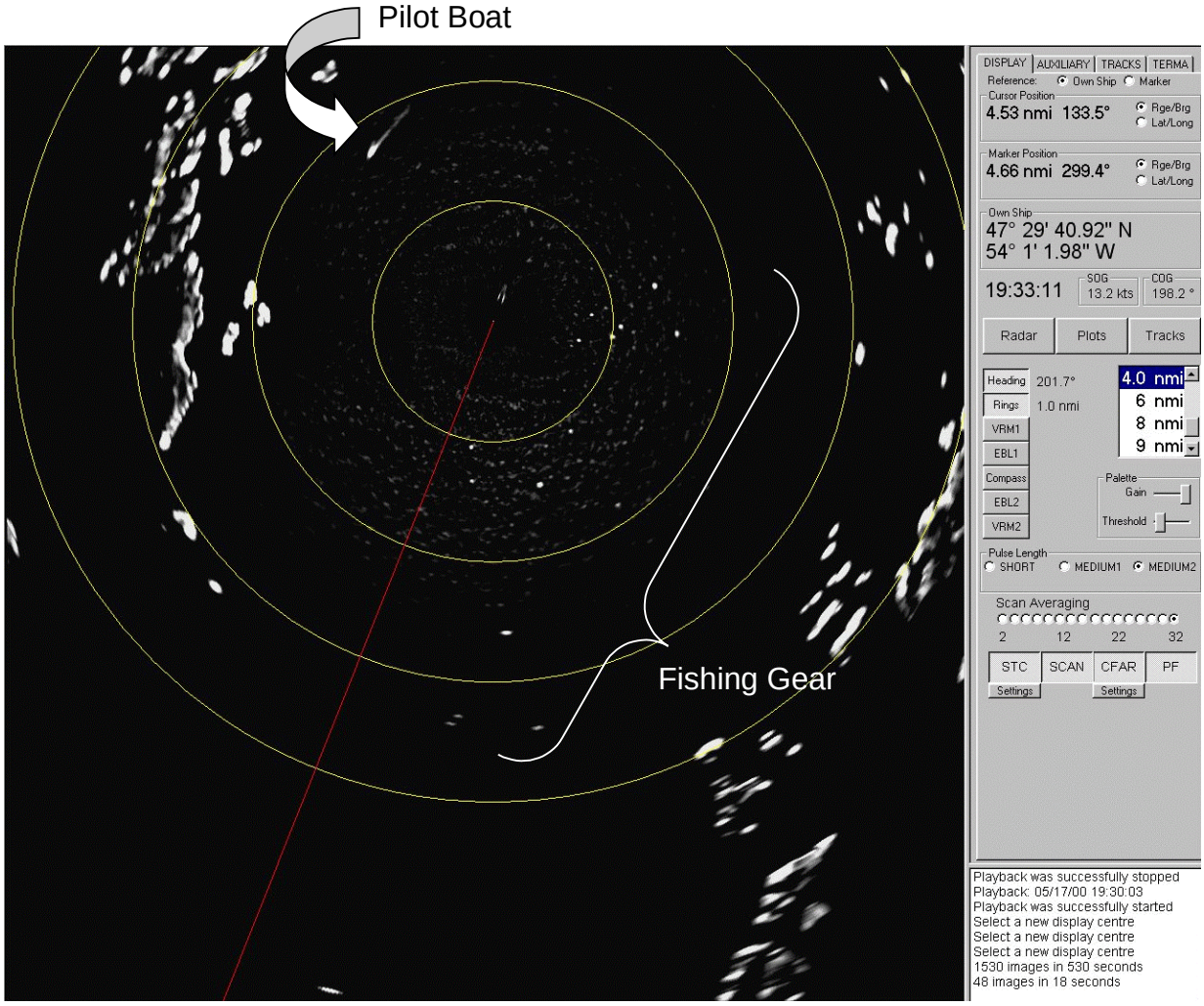

Figure 2: Placentia Bay (processed radar image)

Figure 3 shows data collected as the tanker was approaching the Offshore Loading System (OLS) at Hibernia. Hibernia is the large target west of the vessel. The OLS equipment is submerged, but marked by a surface buoy. This buoy can be seen in the processed image (Figure 4) southwest of the vessel. The wind speed at the time of this data was about 15 kn from a direction of 210°. Swell was estimated at about 2 m with some white caps.

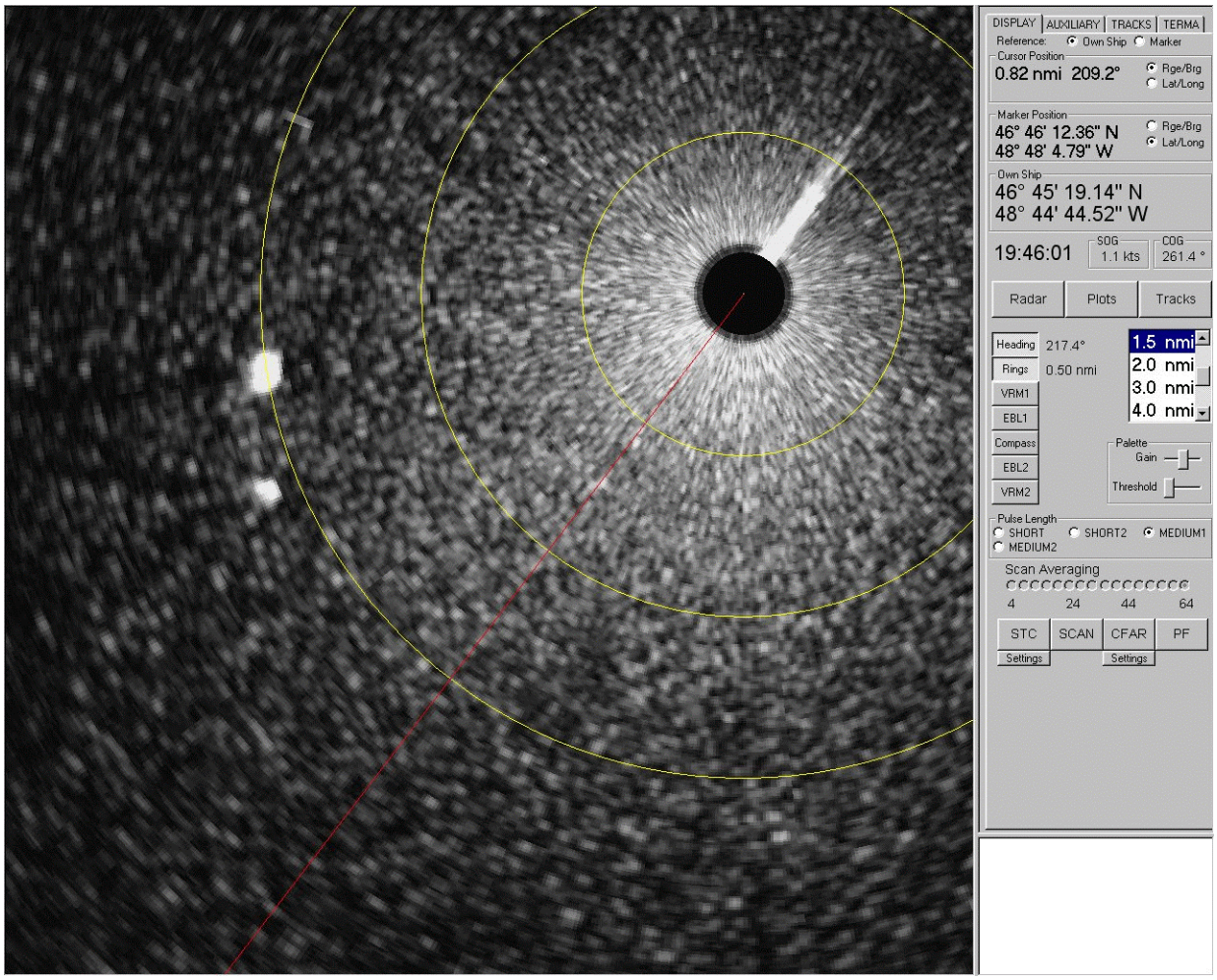

Figure 3: Approaching OLS (unprocessed radar image)

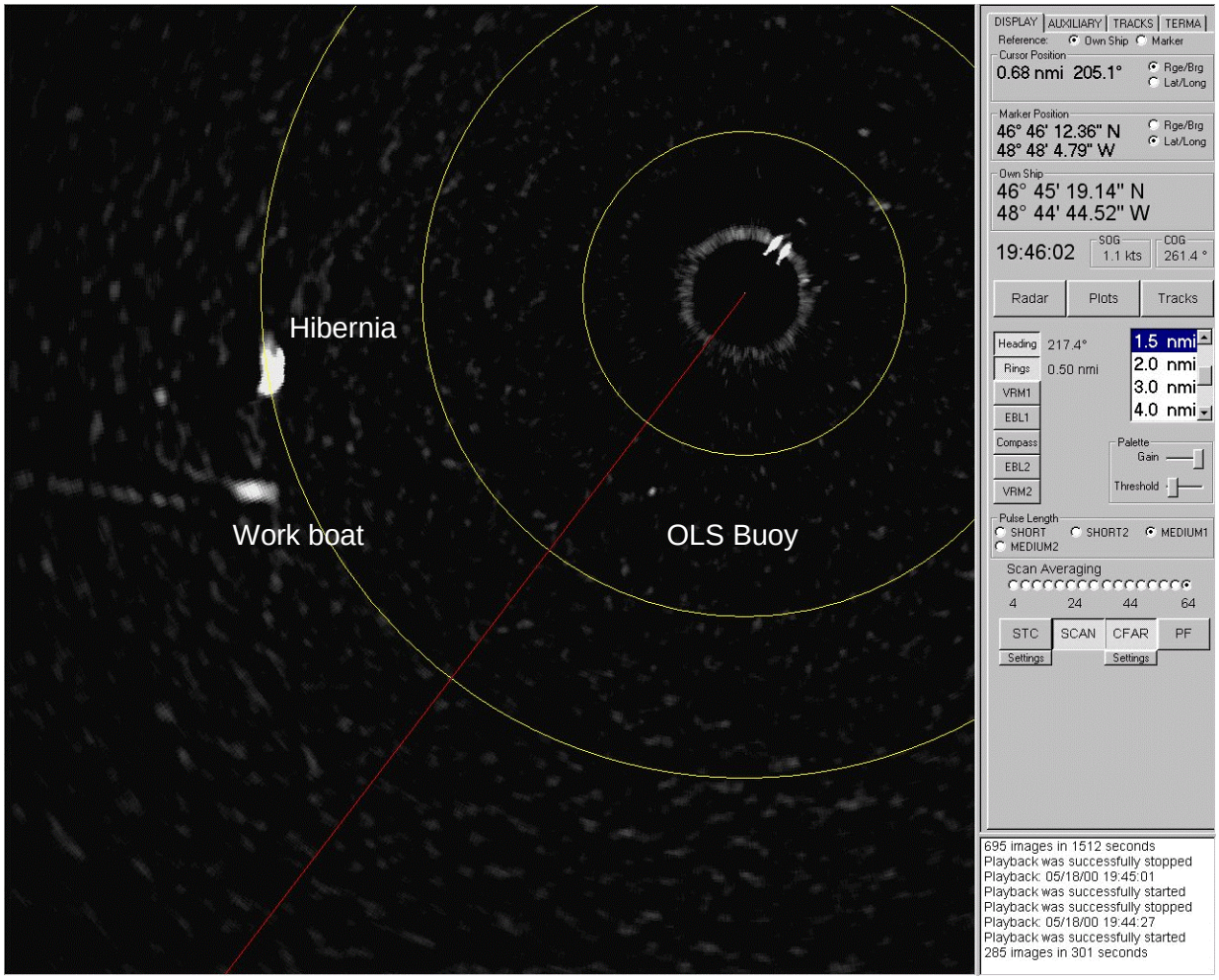

Figure 4: Approaching OLS (processed radar image)

3. DESIGN APPROACH

The rest of this report is dedicated to a review of the development of the RSi4000 radar interface card. The approach used in this design was based on past success in hardware design and fabrication. From the outset, it was understood that the schematic design and PCB layout of the board would be done in close consultation with an outside firm. This process required that a preliminary design be delivered to the consulting firm. After a review of the preliminary design, an electrical interface would be designed by the consultant to meet the input and output specifications. Sigma Engineering Limited would then take full responsibility for developing the on-board logic required to stream the data to the host PC. Once the logic was developed, the full schematics and PCB layout would be developed by the consulting firm. These would once again be reviewed before sending the files off for fabrication. Testing of the board would be done by Sigma Engineering Limited, with the consultant assisting in making modifications as required.

Consolidated Technologies Limited of St. John's, Newfoundland, was chosen as the consulting firm to provide the electrical/mechanical design. Consolidated Technologies Limited had performed a similar role with the previous version of Sigma Engineering Limited's radar interface card.

3.1 Conceptual Design

In the conceptual design phase, block diagrams of the card were generated. The aim of the block diagram was to ensure that all inputs, outputs, and control signals were enumerated from block to block without concern as to how these signals were actually connected internally within the blocks.

Several block diagrams were produced and some common elements began to materialize. These elements included:

- Trigger input and conditioning with programmable delay
- Video input and conditioning with programmable gain and offset
- ACP/ARP input and conditioning
- Azimuth interface from counter, synchro, or parallel word
- Minimal on-board storage with FIFO architecture
- A programmable clock, synchronized to trigger
- On-board logic for data flow control and data consolidation

3.2 Selection of PCI Controller

Before proceeding to the preliminary design, guarantees were needed that the video pulse, once assembled on the card, could be bus-mastered across the PCI interface. To address these concerns it was necessary to review the PCI-bus interface specification and choose a PCI controller to be used by the card. The AMCC S5935 PCI Matchmaker was quickly determined to be the only viable choice; its alternative, the PLX PCI9050 was eliminated due to limits on its support for bus-mastering. Appendix C provides a short description of this chip and its register definitions.

3.3 Preliminary Design

The preliminary design was produced and delivered to Consolidated Technologies Limited for their response. The preliminary design specified the following:

- Use of AMCC S5935 chipset with pull-ups on S5935 control lines as required by the AMCC specification
- Serial EPROM interface for setting the AMCC configuration options.
- On-board buffering consisting of two 16-bit wide FIFOs, each capable of holding a single pulse of digitized video plus the associated header
- Samples to be collected in multiples of 256 at sampling rates as high as 60 MHz
- DACs for setting trigger threshold, video gain and offset, and possibly ARP threshold
- Power regulation for analog section and DAC reference voltages
- Optional azimuth interfaces were to include a counter (for ACP/ARP), a synchro-to-digital converter and a parallel word header
- Counter with 1 MHz clock for measurement of the trigger PRF
- Configurable number of bits in A/D
- Stable, programmable clock synchronized to the trigger input

3.4 Electrical Interface

In response to the preliminary design, Consolidated Technologies Limited reviewed the available A/D chips and selected the AD9226ARS, a 65 MSPS, 12-bit A/D converter. Support for the 8-bit mode could easily be accommodated by discarding the lower 4 bits if desired.

Following approval of the A/D selection, electrical interfaces to the following components of the preliminary design were developed:

- Trigger interface circuit (TTL-out)
- ARP interface circuit (TTL-out)
- Video interface circuit with gain/offset control
- S5935 PCI interface circuit with serial EPROM
- Power regulation
- Counter, synchro, and parallel angle interface
- ACP interface circuit with opto-isolated inputs (TTL-out)
- Programmable DAC outputs
- FIFO interface

A review of the electrical interface resulted in some initial modifications. For instance, the ARP circuit was rejected, and it was decided to use the opto-isolated circuit for both ACP and ARP inputs. Other circuitry requiring proprietary design included:

- trigger delay
- clock synchronization and synthesis

Diagnostic LEDs were also added to the circuit by Consolidated Technologies Limited.

3.5 Logic Synthesis

With the electrical interface proposed, the focus shifted to prototyping the required PLD firmware. By using simulator software with asynchronous clock support, some early prototypes were easily implemented using the 20RA10s device model. As work proceeded beyond the prototyping stage, it became necessary to select a CPLD (Complex PLD) as the target device. The search for a suitable CPLD ended in the selection of the Lattice ispM4A series of CPLDs. These chips had all of the following features that made it ideal for use in this project:

- Programmable without expensive hardware using a JTAG interface
- Programming software with support for the ABEL programming language available at low cost from Lattice
- Sophisticated simulation tools were included in the Lattice software, allowing the logic to be fully tested during development
- Socket-able PLCC format has 32 IOs per device with up to 64 internal macrocells
- Available with propagation delays as low as 5 ns, making them suitable for use with 120 MHz clocks
- Low cost, especially the ispM4A5-64/32-10JC

With the selection of the ispM4A5 as the target device, the layout required for the board's logic quickly took shape. PLD logic for trigger delay and clock synthesis, which required synchronization to the high-speed 120 MHz clock, was developed first. For this logic, the fastest chip in the series (the ispM4A5-32/32-5JC) was used.

The remaining logic needed to work at only the 60 MHz speed of the A/D clock or the 33 MHz speed of the PCI bus. The ispM4A5-64/32-10JC was therefore suitable for all remaining PLDs. The final implementation required four PLDs working in tandem to accomplish the following tasks:

- Receive input from the host PC during configuration
- Count the number of A/D samples collected for the current pulse
- Load and unload the FIFOs with each new trigger
- Select 8 or 12-bit data depending on the mode selected
- Count the ACPs and measure PRF timing
- Detect timing violations among these signals
- Control the LEDs

3.6 Schematic Design and PCB Layout

The pinouts for the six PLDs required by the design were provided to Consolidated Technologies Limited, who then added these to the design along with a JTAG interface. Schematics were then developed and the final design was reviewed by Sigma Engineering Limited. The schematics were approved with only minor revisions, and work was undertaken to position the components and traces on a PCI PCB layout.

3.7 Device Driver Development and Theory of Operation

At this time, a device driver was developed by Sigma Engineering Limited. The driver is based on existing intellectual property of the company. Originally, a Windows NT driver was developed, and compatibility with Windows 2000 was achieved by making a few additions to accommodate Windows 2000 device registration strategy.

The driver was designed to operate the card in a very specific sequence. A prototype development board provided by AMCC, the manufacturer of the S5935 chip, was used to test this sequence prior to arrival of the actual hardware. The AMCC prototype board also supported a loopback DMA mode, making it possible to test DMA bus-master logic under control of the new driver. Consequently, a significant portion of the driver's functionality was developed and tested while awaiting fabrication of the prototype.

4. FABRICATION

The PCB layout files were sent to a manufacturer in order to generate the PCI card. After passing an electrical connection test at the factory, the board was delivered to Consolidated Technologies where the components were stuffed and mounted. The resulting card was then inspected and tested by staff at Sigma Engineering.

4.1 Initial Inspection

The fabricated board is a full-length multi-layer PCI card with power and ground planes. Separate 5 V analog and digital power supplies are used, though both share a common ground plane. The power plane supplies the digital circuitry (Vcc) while the analog section receives power from positive and negative 5 V regulators routed along the signal layers.

The board is populated with the majority of the components on the top layer. Approximately 20 components (resistors, capacitors, and a diode array) are populated on the reverse side of the board. Interfaces to external signals are provided through a variety of connectors, as described below:

- A standard DB15 connector (P1) provides access to TTL inputs and outputs as well as synchro-to-digital converter signals
- A high-density DB15 connector (J1) provides pins for positive and negative sides of the ACP, ARP, trigger and video
- An SMB connector (J2) provides access to an external clock, if desired
- Headers P3 and P3A provide the interface to the JTAG cable used to program the onboard PLDs
- Testpoints are available for examining ground, Vcc, Vdd, Vee, A/D video and DAC outputs as well as the outputs of the trigger, ACP and ARP detection circuits
- Various jumpers and switches control the input impedances, input modes (single-ended or differential), and polarities of the video and digital inputs
- Optional synchro-to-digital converter chip or parallel azimuth word (CVD) interface

Initial inspection of the board involved examining the placement of device footprints, continuity between various ground points, as well as for Vcc, Vdd, and Vee, incorrectly stuffed components and overall quality of the fabrication. When satisfied that the board power supply was safely assembled, and that no defects were detectable, the board was installed in a PC via a bus extender card for initial power-up. The voltage levels on each of the power supply lines were verified and the card was watched closely to check for failing components.

The PC was then allowed to boot under Windows NT, which correctly detected the presence of a new PCI card identified by vendor ID 10E8 and device ID 4750. The driver was installed for the device. The board was tested using the DOS software provided by AMCC in order to verify that PCI operation registers were working properly. This process confirmed that the S5935 chip installed on the card was receiving power and signals properly.

4.2 PCI Configuration

An attempt was made to program the Serial EEPROM to set the PCI configuration and allow synchronous bus-master transfers. Initial attempts failed, and it was discovered that the installed EEPROM was faulty. The PCI configuration space was successfully programmed after the faulty EEPROM was replaced.

4.3 Initial PLD Programming

The board was brought to Sigma Engineering Limited in order to program the PLDs and further test the card. The first step in the programming of the PLDs was to verify the presence and type of each device in the chain. Next, PLDs were programmed incrementally in a manner that allowed independent testing of each component. The PLD firmware for U35, which had been extensively tested using the prototype board from AMCC, was chosen as the starting point. Without the other PLDs programmed, it was expected that the resulting output would be a free-running 2.5 MHz clock. The ADCLK output was examined at various places in the circuit to confirm this.

Next, minimalist firmware was downloaded to the board to accomplish the following tasks:

- Generate a free-running A/D clock
- Hold FIFOs in reset
- Program the onboard IRQ
- Respond to the IRQ by clearing the IRQ and reading the mailbox registers, setting the clock frequency and DAC outputs in the process
- Enter an idle mode until the next system reset/IRQ

Generic DOS software, provided by AMCC, was used to manually configure the board and trigger the onboard IRQ. This confirmed the operation of the PLDs programmed to date.

4.4 Calibration of DAC Outputs

With the ability to control the DAC outputs used for video gain, bias and trigger detection, diagnostic software was used to configure and test the DAC outputs as they appear at testpoints TP5, TP6, TP7 and TP8. A problem was discovered with the filtering capacitors (C78, C76, and C79) at this time. The capacitive load that these presented to the DACs caused oscillation that could only be dampened by electrolytic capacitors. Use of electrolytic capacitors restricted the voltage range of these control lines to positive values only. All the filtering capacitors were eventually removed to eliminate the oscillation. The exception was TP8, the offset control voltage, which was reconfigured to have only positive values of offset.

4.5 Bus-mastering and Additional PLD Programming

The next step in the process was to verify that the AMCC S5935 was properly configured for synchronous bus-mastering. To test this, diagnostic software was used to set the card into a loopback mode, whereby bus-masters to the AMCC (PCI read/host write) are looped back to the host PC (simulating a PCI write/host read). This was attempted and worked as expected.

Additional firmware was downloaded to enable trigger detection, including the trigger threshold and programmable delay. A positive-going 5 V pulse was injected into the system and the trigger threshold was set to C0 (roughly 1.5 V). The output of TP9 was monitored for various settings of programmable delay. As designed, a delay value of 255 acts as a pass-through, generating a trigger matching the input trigger duration and delayed by no more than 5 ns. Other delay values produced a 1.066 μs trigger delayed from the input by up to 4.23 μs in 16.67 ns increments.

At this point, the card was now fully configurable, and should have been responding to triggers by initiating bus-master transfers. The initial attempt at implementation failed. Investigation revealed that the FIFO clock was stopped one sample too early due to the fact that the counter chip in use was counting falling edges of the A/D clock instead of rising edges. The firmware was modified to accommodate this, and it then became possible to test the bus-master transfers.

Several measurements were made on the board to assess how orderly data flow from the A/D card to the host was progressing. An oscilloscope was used to verify that PLDs were asserting signals in deterministic ways according to their intended application. It was also possible to measure the timing of the first A/D clock after a trigger. From these latter measurements, it was determined that at sampling rates of 60 and 40 MHz, a 10 ns delay results, while at all other frequencies a 15 ns delay occurs. Jitter on the clock was equal to one 120 MHz clock period, or 8 ns.

4.6 Analog Video Analysis

Control over the gain and the video now made it possible to test the analog video. Some minor corrections were made to the circuitry, but the sensitivity of the A/D chip made additional debugging of the video from an analog perspective counterproductive. Early digital captures of the video revealed that the oscilloscope probes and test equipment added a significant amount of noise to video. Some additional attention was paid to ensuring that the cables and signal generators in use were not contributing to the video noise prior to deciding to continue the analysis in the digital domain.

4.7 Final PLD Programming

Until this point, the values transferred to the host for ACP, PRF (pulse period) and jumper settings were static values latched during initial power-up of the card. The final step was to download firmware in order to update these fields with every trigger. The LED display was also finalized at this time. A solid trigger or video LED indicates the presence of error-free trigger and video. If the LED is off constantly, it indicates the absence of any valid video or trigger voltages (possibly due to mismatch in the settings for gain, offset or trigger threshold). An LED flashing at the rate of 4 Hz indicates that valid video and/or triggers are being detected, but that the current configuration (gain, offset, collected samples) is causing some of the video and/or triggers to be lost. Intermittent flashing of the trigger LED indicates that the host PC is having trouble keeping up with the data throughput. The trigger LED also flashes whenever the host PC reconfigures the card.

4.8 ACP and ARP Detection

At this point, it was possible to connect an ACP and ARP to the card. Jumpers had to be installed on JP5 and JP2, and all switches of S1 were set to the ON position. A 1 Hz signal was input to the ARP and a 1 kHz signal was input to the ACP. The output of the detection circuitry was monitored at various points. It was determined that the detection circuitry lengthens the pulses by tens of microseconds. Additionally, turn on and turn off times for the opto-isolator and output transistors led to some bizarre timing relationships between voltage, frequency and duty cycle of these signals.

A detailed analysis of the behaviour of this circuit was undertaken, as described in Appendix A. The circuit recommended for use on the ACP and ARP in the final design should be modified to have a high-speed configuration with a 620 Ω load resistor and a 6.8K pull-up resistor. The input resistor should be changed to 3.1K. The performance of such a circuit should support low-voltage RS422 at 10 kHz, and faster inputs (50 kHz to 250 kHz) at voltages of 2.68 V or higher.

For both the ARP and ACP, a 150 nF capacitor can be added in-line with the circuit to provide filtering of DC offsets and to provide a capacitive load where required, provided that the differential input voltage exceeds 6.8 V.

5. INTEGRATION INTO SEASCAN

With a varying ACP, the SeaScan software could now be used to display the video in scan-converted format. Modifications were made to the SeaScan system to support capture using the RSi4000-RT-8/12 in both 8-bit and 12-bit modes. For the 8-bit mode, the only required change was to use an alternate A/D capture DLL, named RSi4000RT.DLL. In addition to accessing the data from the RSi4000-RT-8/12 driver, this DLL also contains an entry point that replaces the configuration program used in previous versions of SeaScan.

For the 12-bit version of the program, the following executables needed changes to support the larger image sizes:

- SeaScan.EXE
- SigmaIMG.DLL
- SigmaPLT.DLL
- SigmaTape.DLL
- SeaView.EXE
- SU4000.EXE (formerly SampleClient.EXE)

The new versions also provide more stable azimuth gating algorithms, and better record and playback performance.

5.1 Trigger Calibration

SeaScan was configured to allow sampling at 2.5 MHz, 7.5 MHz, 10 MHz and 20 MHz, depending on trigger period. The trigger period was set to produce a 2.5 MHz image, and a pulse was injected to the video input. The falling edge of the pulse was adjusted so that it was possible to see the transition on the scan-converted image. The pulse period was then changed to compare the location of the falling edge at higher frequencies. Using this procedure, a two sample offset was found to exist in the video. The PLD code was modified to provide the proper sample alignment. The procedure was then repeated and the falling edges of the pulse were aligned within the measuring accuracy of the SeaScan software.

5.2 Digital Video Analysis

Additional analysis of the received video was performed using the diagnostic software (known as the “Status Monitor” or StatMon). This RunDLL32 entry point is available from the RSi4000RT.DLL. It supports pasting of video pulses, in text format, between the RSi4000-RT-8/12 and a spreadsheet application such as Quattro Pro.

Fourier analysis was performed using data in the format of 32 pulses x 2048 samples, set by the Status Monitor menu option. It was determined that the system noise was:

a) wide-band
b) attenuated to -80dB from the nominal DC level

Many existing cards have difficulty digitizing the initial video samples following a trigger, so special attention was paid to the early part of the video to identify whether any corruption was occurring. One phenomenon noticed from the digital video was the presence of an 80 MHz ripple in the first 125 ns (19 m) of video. The ripple is not associated with the input trigger since it is completely independent of the programmable trigger delay. It may be associated with generation of the SYNC and associated reset of the A/D clock that occurs simultaneously with the collection of the first A/D sample. In any case it is a distinct, repeatable signal that causes additional noise in the first few samples at sampling rates of 20 MHz and above. The worst case occurs at 40 MHz, which samples the peak of the ripple on the first (0 range) sample. Because the effect is significantly reduced after the first 10 m and is confined to the first 19 m, it is not considered a significant problem from a radar perspective.

5.3 System Throughput

The host system used throughout the development of the RSi4000-RT-8/12 was a Pentium 2 system, equipped with a 350 MHz processor and 128 MB RAM. The following discussion is based on testing with this system.

The final check of the system was to determine the maximum sustained throughput of the system, especially at high PRFs. Concern about this was raised when, during collection of 2048 samples at 40 MHz, the software reported buffer runouts at PRFs as low as 1333 Hz. (Runouts occur when the buffer is not released by the application software in time for the driver to restart DMA in its interrupt service routine.) Since the application software is only concerned with performing data integrity checks and memory copies at this stage, it should have had ample time to transfer 2048 samples at 1333 Hz. Investigation into the matter concluded that the bottleneck occurred because the data was being copied from a special form of system memory shared simultaneously by the application, driver and bus-mastering device. While access to this memory is fast enough for data integrity checks, a heavy penalty is paid when accessing video through this process. To solve the problem, a ReadFile routine was added to the driver to request that the driver perform the copy on behalf of the application software. This restored normal memory throughput and allowed the system to transfer 2048 samples in 12-bit mode at PRFs as high as 4000 Hz. Switching to 8-bit mode doubled the maximum PRF to 8 kHz. Consequently, the system can sustain core data processing at a rate of 16 MB/s.

The buffer size allocated by the driver is configurable, with a default size of 4 MB. This buffer is requested during the booting procedure of the PC. The large driver buffer relaxes the expiry time of data stored within the buffer – the application level software has twice the number of timeslices available to it for scheduling than it does when using the smaller buffer size. The result is improved throughput over and above that using the default buffer size. In this mode, the system can transfer 2048 samples in 12-bit mode at PRFs as high as 6000 Hz. Switching to 8-bit mode doubled the maximum PRF to 12 kHz. Consequently, the system can sustain core data processing at a rate of 24 MB/s when 4 MB buffers are used.

These results were obtained on a development platform consisting of a Pentium 2 motherboard with a 350 MHz processor. Later testing on Pentium 4 platforms gave data capture rates up to 56 MB/s.

6. CONCLUSIONS

In summary, the tasks undertaken during this project were:

1) **Conceptual Design**: Generation of block diagrams to enumerate all inputs, outputs, and control signals necessary.
2) **Selection of PCI Controller**: Detailed analysis of the signals and timing constraints specific to the PCI bus.
3) **Preliminary Design**: Submission of a proposal to a consulting firm to procure an implementation of the electrical interface.
4) **Electrical Interface Review**: A cost-benefit analysis of the circuitry proposed, and an assessment of the logic necessary to coordinate the signals and data produced by each interface.
5) **Logic Synthesis**: Design and simulation of the necessary logic in order to prove the feasibility of the design.
6) **Schematic Design and PCB Layout**: The final electrical interfaces and all required logic are documented and PCB Gerber files are produced for fabrication of the board.
7) **Device Driver Development and Theory of Operation**: A driver is produced that implements the PCI-host side of the required logic. Initial diagnostic software is also produced that operates on simulated data flow from the driver.
8) **Fabrication**: The Gerber files and components are sent for manufacture into the prototype board.
9) **Initial Inspection**: Issues related to board construction are documented. The board is inspected for proper configuration of the power supply. Finally, the board is installed in a PC to verify proper operation of the PCI interface.
10) **Configuration**: The board is configured for testing.
11) **Initial PLD Programming**: The JTAG interface is checked by polling the IDs of the installed PLDs. The PLDs are then programmed in stages (where possible) to test the operation of the PLD in isolation from each other.
12) **Calibration of Analog Signal Control Lines (DAC Outputs)**: Application software is tested with the actual hardware. The card is set to various configurations and the result of the configuration change is examined at the analog level to fully test the operation of each of the installed chips on the board.
13) **Bus-mastering and Additional PLD Programming**: PLD code is enabled to allow data to flow into the FIFOs and out to the PCI interface. Application level software is also finalized to display the captured data.
14) **Analog Signal Analysis and Final PLD programming**: The final version of all the PLD code is sent to the card and any untested analog interfaces are fully examined.

15) **Integration into SeaScan**: The resulting hardware is integrated into the mainstream product.
16) **Trigger Calibration, Digital Video Analysis, and System Throughput**: The system is fully characterized in order to quantify its performance in comparison to the previous versions.

This report has chronicled the decisions made in each step above that had an impact on the success of the project. It focuses largely on problems with the hardware, firmware, and software that were discovered at each stage and corrected. While there were many modifications made to the board and source code over the course of the development, this was to be expected as part of a new design. The end result is that the behaviour of the card has been fully investigated and is well understood by staff at Sigma Engineering Limited.

The final card produced by the process documented in this report has been a resounding success. The card has been extensively tested, and where problems have been found, they have been corrected by revising the original component values, or by modifying a PLD. Consequently, no visible modifications were required to the prototype to make it suitable for production. In the process of testing the hardware, the mainstream version of the software was also thoroughly tested and improved.

Appendix B describes the specifications of the final card based on the default configuration of the board as shipped by Sigma Engineering Limited. This specification is suitable to interface to the majority of radar systems. The knowledge gained through the development process about its operation makes it possible to alter the factory default configuration as needed to support radars outside of this specification.

7. RECOMMENDED CHANGES FOR BUILD 2

Physical Layout

1) Correct the footprint for the AD9226 A/D chip.
2) Increase spacing between C34 and C28.
3) Adjust footprint for J1 to ensure proper fit to faceplate.
4) Add a shield ground to the DB connectors (P1 and J1).
5) Connect pin 1 of P1 (IN-MB7) directly to GND.

DAC Outputs

1) Do not stuff R55 and set R61 to 8K to yield an offset range of 0 to 3 V. Change the value of R55 to 12K on the schematic.
2) 250 kHz oscillation occurs due to noise on 12 V input. Do not stuff filtering caps C75, C76, C79, and C1. OK to stuff C77 and C78.
3) Change the value of R36 to 1.5K and R39 to 10K on the schematic.

Analog Video

1) Correct the polarity of C17 and C18 on the schematic and the silkscreen so that the positive terminals go to CAPT and the negative terminals go to CAPB.
2) Replace C16 with an 18 Ω resistor.
3) Change the voltage divider at the front end of video to a 3:1 ratio (R25=2K, R25A=2K).
4) Add space for a low-pass filter capacitance in parallel with D7. The capacitance should have a value of 150 pF.
5) Route the video along the reverse side of the board to isolate it as much as possible from the digital signals.

Digital Video

1) Digital video shows some ringing in the first 19 m. Worst case sampling appears to be at 40 MHz where the peak of the overshoot is sampled by the first (range 0) sample. Investigate possible sources of this noise and remove if feasible.
2) Fourier analysis of video collected at 40 MHz shows white noise limited to -80 dB. Spikes can be seen at 10 MHz, 15 MHz, 18 MHz and 19 MHz; however, the amplitude of these spikes is still relatively small.
3) The falling edge of the input trigger creates a noise spike on the video with amplitude of four digital levels at unity gain.

Synchro Interface

1) Mark "(MSB)1" on silkscreen next to pin 1 of U18. (Rotate text so it appears upside-down.)

2) Correct header H1 so that jumpers can be used in horizontal position for re-routing RH and RL.

ACP/ARP Interface

1) Add 6.8K pull-ups to 2N3906 transistors, and change resistor value at the collector of these transistors to 620 Ω.
2) Add space for an optional inline component on the input, to be stuffed with either a 100 to 150 nF capacitor, or a 0 Ω jumper.

Other Notes:

System Throughput

1) In the 2 MB driver buffer configuration, the single card throughput is slightly more than 16 MB/s. This is adequate for the collection of 4096 16-bit samples at 2 kHz PRF, or 2048 8-bit samples at 8 kHz PRF. For marine radars operating at 3 kHz, the number of samples collected in 16-bit mode is limited to 2560, representing a range of 5 nmi at 40 MHz.
2) For single card systems with 4M buffers allocated at boot time by the driver, the system throughput can be increased to 24 MB/s.

Range Calibration

1) Simulation of the PLDs showed that video delay for 60 and 40 MHz would be less than the delay for lower frequencies. This was confirmed by measuring the position of the first stable A/D clock after a trigger.
2) With the DELAY PLD operating in passthru mode, the measured delay for 60 MHz and 40 MHz frequencies was 28 ns (4.2 m). For all other frequencies, the delay was nominally 33 ns (5.0 m). 18 ns of this delay is due to propagation delay between the input and output trigger.
3) With the DELAY PLD programmed for zero-delay, an additional propagation delay between input and output triggers of 10 ns is added.
4) Jitter on the clock is limited to 8.3 ns with typical values around 6 ns.
5) Based on the results of the delay measurements, we can expect the video to be offset on average by 5.0 m [((33ns+6ns)+28ns)/2] with a correlation of +/- 0.975 m [((33ns+8ns)-28ns)/2] from one pulse length to the next in passthru mode.
6) We can add delay from 2.5 m to 637.5 m (16.6 ns to 4.25 μs) in 2.5 m increments. In this case, the video will be offset on average by an additional 4.0 m [((33ns -6.6ns+6ns)+(28ns-6.6ns))/2] from the expected delay value. Correlation between pulse lengths remains the same at +/- 0.975 m.
7) The video subsystem can be calibrated on a per-frequency basis in order to obtain a maximum target jitter of +/- 0.6225 m.

Software and Firmware

1) Firmware developed in Build 1 was modified slightly from its original source in order to improve the operation of the board. The most significant changes stemmed from the fact that U25 counts the falling edges of the A/D clock instead of the rising edges. As this actually improves timing relationships, the changes to the PLD are all that are necessary to correct for this. Other PLD changes include minor modifications to the LED status indicator logic and measurement of pulse period. It is anticipated that the current version of firmware will be suitable for future builds without modification.
2) Software developed for the RSi4000-RT-8/12 includes a Windows NT driver, several diagnostic utilities, and a DLL for use with the SeaScan software. The interface to the driver consists of three calls that will be documented in a help file to be delivered with the DLL. A Windows 2000 version of the driver is also available.
3) Support for two or more cards installed in the current PC should be incorporated into the delivered software.

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APPENDIX A: ANALYSIS OF ACP/ARP DETECTION CIRCUITRY

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ANALYSIS OF ACP/ARP DETECTION CIRCUITRY

Circuit Operation

The RSi4000-RT-8/12 uses opto-isolator circuits to detect ACP and ARP pulses. These circuits have special input and output relationships that can be difficult to characterize, especially in terms of the frequency response of the circuit. The simplest method for describing the operation is therefore to characterize the DC behaviour, and then study how this behaviour changes based on AC parameters.

DC Characteristics

From a DC perspective, the circuit is best described as a voltage-controlled voltage-source. Any voltage above 0.7 V at the input drives a current through a 4.7K resistor into an input LED. The current passing through the LED allows a proportional current to flow through the opto-coupler output. A 2N3906 transistor magnifies this output current and uses it to drive a load resistor. The load resistor converts the current into the output voltage.

The first test of the circuit was to determine what value of input voltage maps into a logic high (approximately 4 V) on the output. For a load resistance of 4.7K, an input voltage of 1.29 V is sufficient to produce a logic high at the output. For a load resistance of 620 Ω, the threshold voltage increases to 1.9 V.

If 6.8K pull-up resistors are added to the base of the 2N3906, the threshold voltage increases to 2.59 V for a load resistance of 4.7K, and 2.47 V for a load resistance of 620 Ω.

Low Frequency Characteristics

Using the DC thresholds as the reference input, the low frequency behaviour was investigated. The pulse generator was set up to produce a 1 Hz signal. The signal polarity was varied as needed to measure the on-time and the off-time of the detection circuit.

With the input voltage set to the threshold voltage, the on-time for a 4.7K load was 70 µs, while the off-time was 100 µs. The values improved by 50% for a load resistor of 620 Ω, with the on-time being 26 µs and the off-time being 50 µs.

Effect of Increasing Voltage

The effect of increasing the input voltage beyond the threshold levels is:

1. on-time dramatically shortens
2. off-time lengthens

The following table indicates the results obtained for the two circuits tested:

no pull-up		Vin=Vth		Vin=3.55 V	
Rl (Vhi)	Vth	Ton	Toff	Ton	Toff
4.7K(2.5 V)	1.07 V	411 µs	7 µs	4.8 µs	59 µs
4.7K(4.0 V)	1.29 V	100 µs	41 µs	7 µs	220 µs
620 (4.0 V)	1.9 V	26 µs	50 µs	7 µs	50 µs

Effect of Pull-up Resistor (high-speed configuration)

When a 6.8K pull-up resistor was added to the base of the 2N3906, the result was to dramatically lengthen the on-time and dramatically shorten the off-time. Once again, the effect of increased voltage was noted to be a dramatic reduction in the on-time and an increase in the off-time. Note that in this case, increasing the voltage more than compensates for the negative effect the pull-up has on the on-time; consequently, exceptionally good high-speed performance is possible in this configuration at voltages of 3.55 V and above.

6.8K pull-up		Vin=Vth		Vin=3.55 V	
Rl (Vhi)	Vth	Ton	Toff	Ton	Toff
4.7K(2.5 V)	2.6 V	72 µs	0.12 µs	16 µs	2.30 µs
620(2.5 V)	2.5 V	48 µs	0.22 µs	12 µs	2.30 µs

The question arises: what is the optimal input voltage for the circuit? To determine this, the voltage applied to the test circuit was increased until the low-frequency (1 Hz) on-time equaled the off-time. The point at which this occurred was 6.5 V, at which point both the on-time and the off-time were 3.85 µs. For input voltages less than 6.5 V, the

on-time will be greater than 3.85 µs and the off-time will be less than 3.85 µs. The opposite is true for voltages greater than 6.5 V.

High Frequency Characteristics

The high frequency characteristics of the circuit are not fully known other than to comment that as the frequency increases, the on-time will decrease while the off-time will stay nominally the same. For example, when a 4 kHz, 3.55 V ACP is input to the high-speed configuration with a 4.7K load resistor, it has an on-time of 13.1 µs compared to 16 µs for the 1 Hz signal.

Practical Considerations

Some concern still exists regarding the ability of the circuit to be driven by real-world signals such as the Bridgemaster ARP signal and by RS422-signals. Based on the results of the testing, it is possible to recommend modifications to the design to support these cases.

For RS422 signals, the main impediment to detection by the high-speed circuit is the 2.5 V threshold voltage. RS422 signals may have differential inputs as low as 2.0 V. Since in reality it is the threshold current, not the voltage that acts as the mechanism for signal transfer, we can support 2 V signals by lowering the input impedance. The threshold current at 2.5 V in the original circuit is computed to be (2.5-1)/4.7K, or approximately 0.32 mA. To produce this current at 2 V, we should reduce the input impedance to (2.0-1)/0.00032, or 3.1K.

The problem with the Bridgemaster ARP is that, in the past, it has been shown to want a capacitive load. By inserting a capacitor inline with the ARP input, we can satisfy this requirement for the Bridgemaster and similar cases. In conjunction with the 4.7K input resistor, the capacitor will act as a voltage divider for the frequencies passed. To minimize the voltage drop on signals of interest, we want to choose a capacitance that results in less than 1/4 attenuation for pulses with a duration of 1 ms or less. This means the reactance of the capacitor at 1 Hz must be 1.6K (1/3 the 4.7K input resistor value). This corresponding capacitance is 100 nF. The resulting circuit was tested and successfully detected pulses as small as 10 µs when the input voltage was greater than or equal to 6.8 V.

When the input impedance is changed to 3.1K to support a lower threshold, the inline capacitor should be increased accordingly to yield a reactance of 1K at 1 kHz. Repeating the equations results in a new value of 150 nF.

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APPENDIX B: FINAL SPECIFICATIONS FOR RSi4000-RT-8/12

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SUMMARY OF RSi4000-RT-8/12 FEATURES

The RSi4000-RT-8/12 interfaces to commercial radars with the following specifications:

Radar Trigger	
I/O Modes:	single-ended
Absolute Voltage:	-25 V to 25 V
Maximum PRF:	32 kHz
Input Impedance:	75 Ω or Hi-Z
Programmable Delay:	up to 4.25 µs in 16.66 ns increments
Hardware Compression:	Optional 2:1
Video	
I/O Modes:	single-ended or differential, 8-bit or 12-bit
Absolute Differential Voltage:	-10 V to 10 V
Bandwidth:	30 MHz
Input Impedance:	75 Ω or Hi-Z
Sampling Rates (MHz):	60,40,30,20,10,7.5, 5 and 2.5
Supported Pulse Lengths:	33 ns to 40 µs
ACP/ARP Configuration:	
I/O Modes:	single-ended, differential, and RS-422
Input Impedance:	75 Ω or Hi-Z
Absolute Differential Voltage:	-5 V to 5 V for 75 Ω @ 50% duty cycle; otherwise -25 V to 25 V.
Required Duration:	22 µs worst case, 4 µs typical
Parallel Angle/CVD Configuration:	
I/O Modes:	12-bit TTL-level I/O
Handshaking:	Assert 2-µs CB signal during data transition
Connector:	14-pin male ribbon cable mounted on-board
Synchro Configuration:	
Converter Resolution:	4096 counts = 360 degrees
PCI-bus Interface:	
Card-to-Card Throughput:	66 MB/s
System Throughput:	24 MB/s (when using SeaScan/RT software)
DMA Buffers:	2 to 4 MB allocated from Host RAM
Drivers:	Windows NT, Windows 2000
Diagnostic Utilities:	Error Logging and Sample Capture Utilities
Client/Server Software:	SeaScan server with Seaview client display Optional tracker software and OEM interface

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APPENDIX C: AMCC S5935 REGISTER DEFINITIONS

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The S5935 chip is developed by AMCC in order to simplify the development of PCI hardware. The chip contains all the circuitry required in order to initiate and service I/O requests between the host PC and the PCI hardware. Bus-mastering requests to and from the card are fully supported. A full description of the AMCC S5935 chipset and its capabilities is available in “The PCI Products Data Book S5920/S5935" available from AMCC’s website http://www.amcc.com.

The AMCC S5935 contains four outgoing mailbox registers (v1OMB0 to v1OMB3), each with four bytes of data that can be written by the host PC and read by the RSi4000-RT-8/12 hardware. Table C-1 gives the details of the register assignments.

Video Offset TP8 (v1OMB2[3]):

Register Value	Video Offset Voltage
0-255	0 to 3 V (desired = 2V dc)

Video Gain TP7 (v1OMB2[2]):

Register Value	Nominal Video Gain
0-255	0x to 1x (desired = 2V p-p)

Trigger Threshold TP6 (v1OMB2[1]):

Register Value	Trigger Threshold
0-255	-2.5 to +2.5 V

Video Offset TP5 (v1OMB2[0]):

see v1OMB2[3] for details

TTL Output (v1OMB1[3]):

Bit	Function
bits 7-2	reserved;
bit 1	Pin9 of DB15M (0=0V, 1=5V)
bit 0	Pin10 of DB15M (0=0V, 1=5V)

Frequency Select (v1OMB1[2]):

Divisor	v1OMB1[2]	Frequency (based on 120MHz clock)
2	00-1F	60
3	20-3F	40
4	40-5F	30
6	60-7F	20
12	80-9F	10
16	A0-BF	7.5
24	C0-DF	5.0
48	E0-FF	2.5

Programmable Delay (v1OMB1[1]):

Register Value	Time Delay
0-254	0 - 4.23us in 16.67ns increments
255	bypass mode (no delay)

Pixel Count (v1OMB1[0]):

Register Value	Collected Samples
0-7	256 samples
8-15	512 samples
16-23	768 samples
24-31	1024 samples
56-63	2048 samples
120-127	4096 samples (limit for 12-bit mode)
248-255	8192 samples
V	((V/8)+1)*256
((S/256)-1)*8	S

Table C-1 : Registers v1OMB1 and v1OMB2

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APPENDIX D: NEW IDLER GEAR INSTALLATION

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ANALYSIS OF ANTENNA TRACKING ERROR IN RAYTHEON MK2

In the 1997 field trials on the CCG *J.E. Bernier*, an error in the angular position of targets was noted. Upon further analysis, the error was found to be sinusoidal in nature, having three cycles (minima/maxima) for every two scan period. An error correction curve was created to compensate for the variation. The intent of this curve was to restore the reported angle to its true position. The curve was generated in software using the following procedure:

1. Buffer data from a binary dump of the antenna angles
2. Segment the buffered data into multiple arrays, with each array representing a 2-scan block of data. The angles were adjusted in the second scan by adding the maximum ACP count to them. In the ideal case, this would generate a smooth ramp varying twice the ACP count in height (e.g. 0 to 8191).
3. Generate 2-scan error correction curve for each block of data by subtracting the idealized ramp from the input data.
4. Scale all resulting 2-scan error correction curves in length to a nominal length matching the number of pulses that would occur in a 2-scan period at the specified PRF.
5. Average the normalized 2-scan error correction curves together to produce the final curve used in the application.

It was deduced that the one-and-one-half cycle per scan sinusoidal error curve was related to the idler gear, which rotates with a 3:2 gear ratio with the antenna and encoder. The mechanism for how the idler gear contributes to the error can best be explained by visualizing two diametrically opposite teeth (A and B) on the idler gear. On the first scan, these pass by the encoder in the order ABA. On the second scan, these pass by the encoder in the order BAB. Any machining or mounting errors that cause teeth A and B to be slightly less or slightly greater than half the diameter of the gear will be detectable by comparing one scan to the next.

Under contract to TDC, Sigma Engineering Limited arranged to have the idler gear removed and replaced.

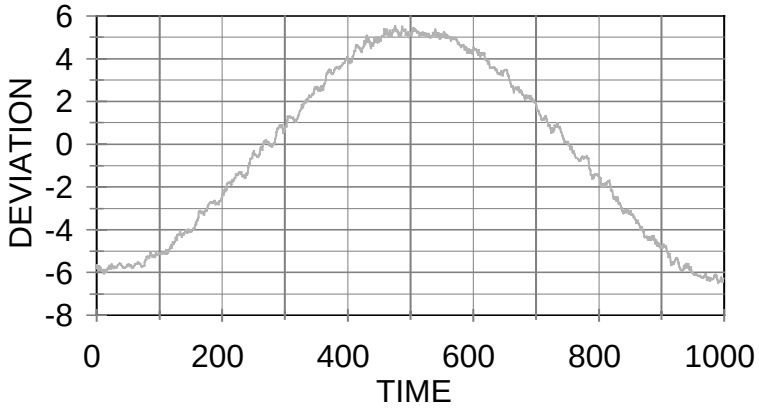
Analysis software was created in order to determine the effectiveness of the idler gear replacement. The source code used in the generation of the error correction curve was modified to provide some interactive controls. Additionally, it was noted that the requirement for the software was no longer to produce a correction curve. Instead, the requirement was to determine the overall effect of the errors both visually and on processing algorithms. To meet this requirement, the following steps were added to the existing algorithm:

1. The point-to-point angular deviation was measured by subtracting the second scan (BAB) from the first scan (ABA).
2. The first two thirds of the resulting curve (AB-BA) is a map of the deviations transferred by the gear from one rotation to the next.

Curves were generated for the original gear and the new gear. The following results were obtained:

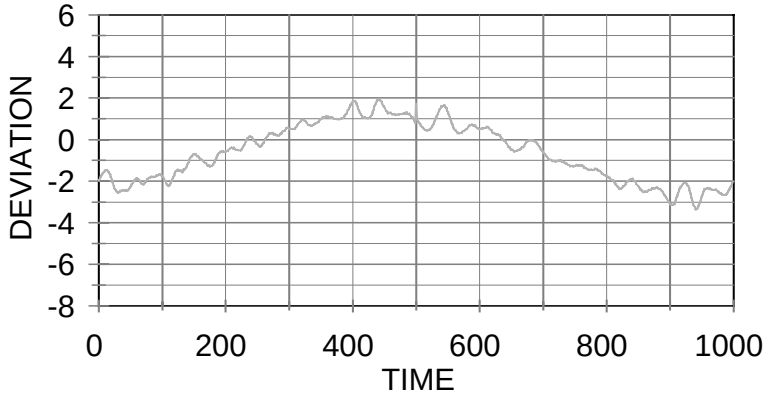
Original Radar

Error curve (AB-BA)



Corrected Radar (Mar 2000)

Error curve (AB-BA)



Conclusions

In the original radar, the maximum deviation between any point and the corresponding point in the previous scan was strongly dominated by a sinusoidal function that contributed the bulk of the error. For a significant percentage of the image, the deviation exceeded 3 ACP counts out of 4096, or 0.26 degrees. The corrected shows a significant reduction in the effect of this sinusoidal function, being dominated by high-frequency variations with amplitude of +/- 1 ACP count. The error is limited to less than 3 ACP counts out of 4096 for the entire rotation. This means that, in the corrected radar, the measured location of the target on the screen varies by no more than +/- 1.5 ACP counts from its apparent (true) position (+/- 0.13 degrees).