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CANADIAN PHOTONICS FABRICATION CENTRE
CENTRE CANADIEN DE FABRICATION DE DISPOSITIFS PHOTONIQUES

NRC · CNRC | Carleton UNIVERSITY

Metrology Challenges in Nanofabrication of Photonics Devices

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CPFC: Lighting the Future

CCFDP : Pleins feux sur l'avenir

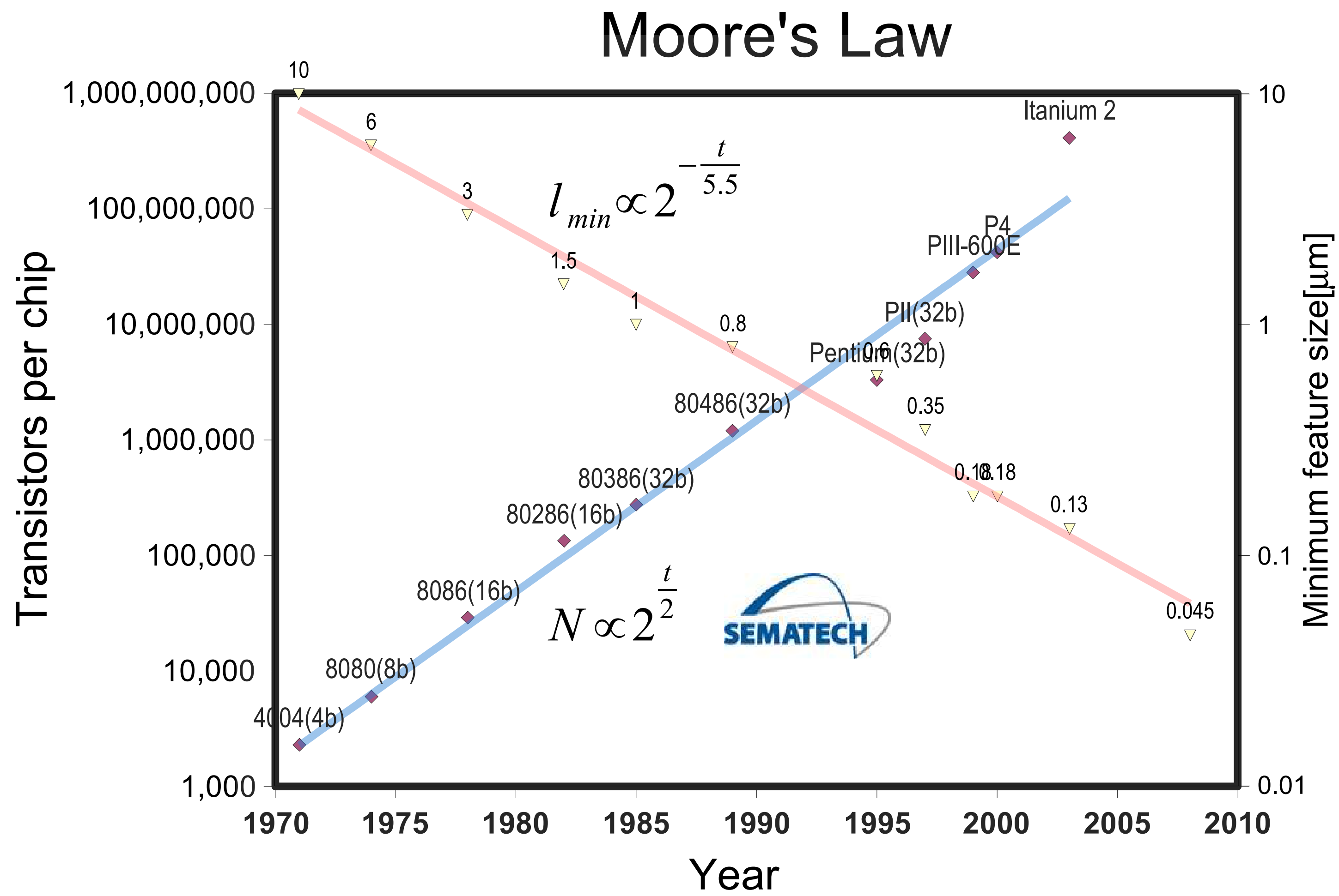
7-Feb-2007

Canada

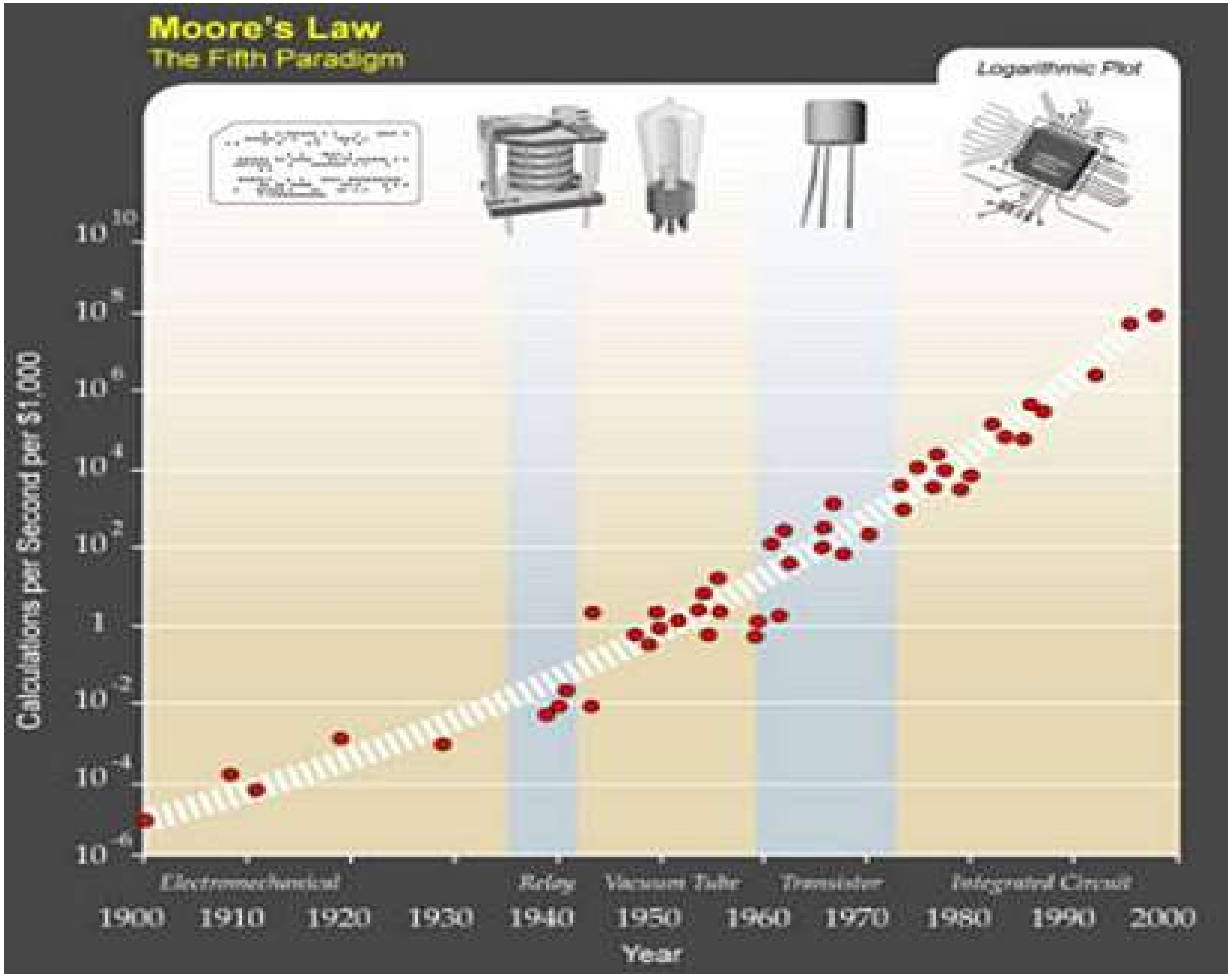
Talk outline

- Downscale trend in electronics Moore's Law
- Downscaling in photonics. Device examples.
- Challenges of photonics fabrication at nm scale
- Metrology in nanophotonics fabrication
- Methods of reference specimens fabrication
- Reference sample fabrication at CPFC
- Closing comments

Moore's Law works for almost 40 years!



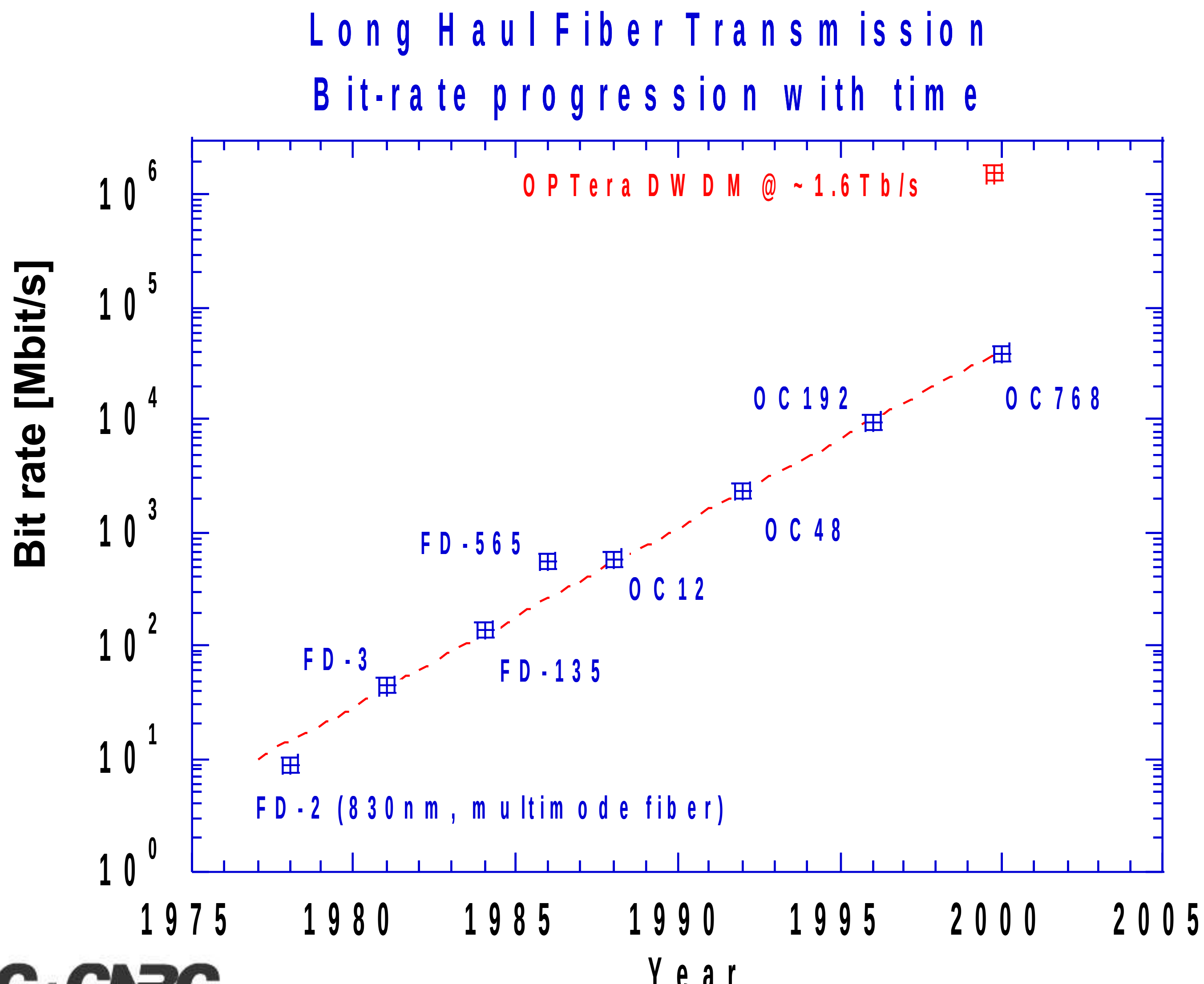
Moore's Law from a consumer perspective



CPFC:
Lighting
the Future

CCFDP :
Pleins feux
sur l'avenir

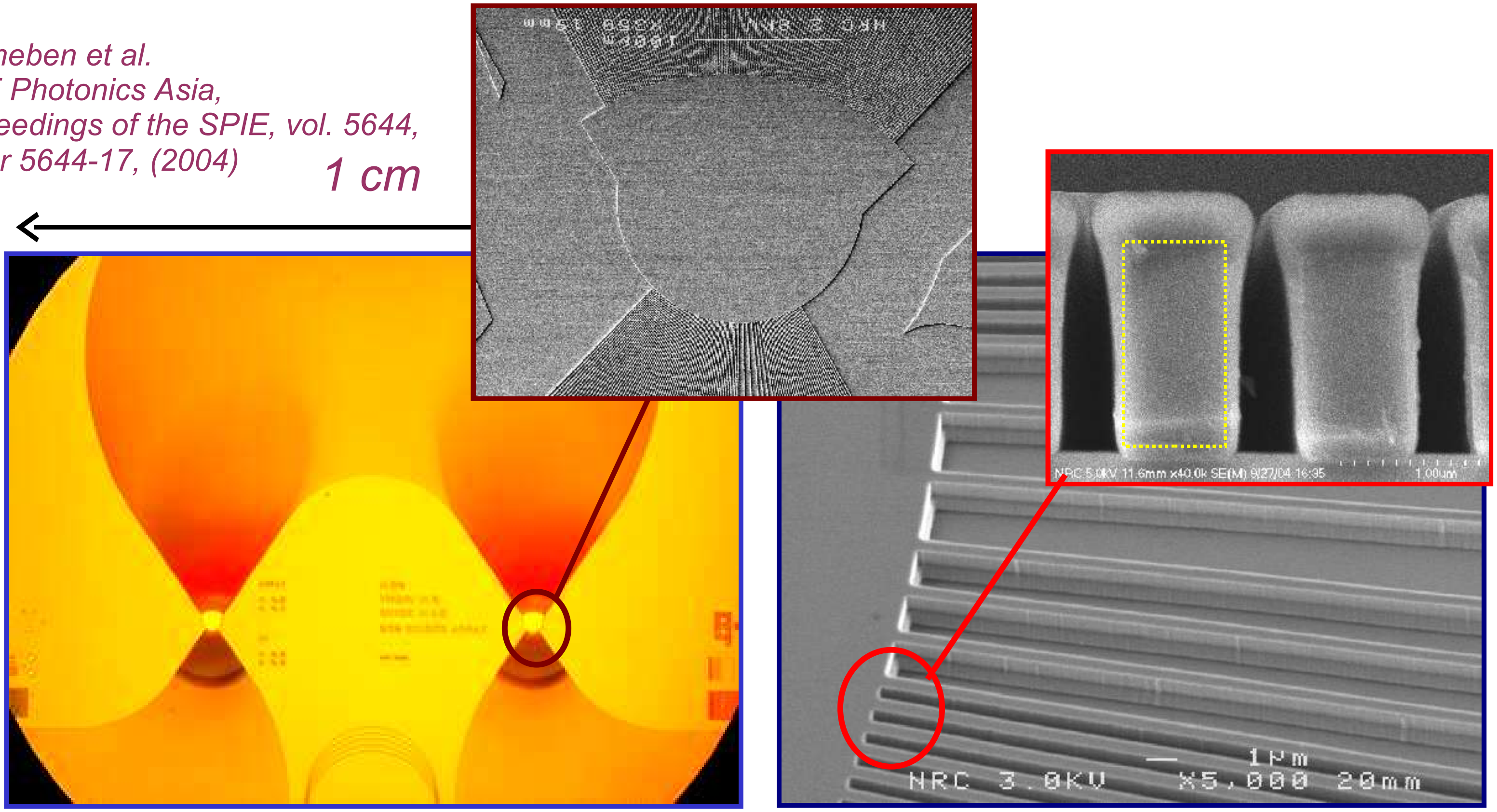
Performance trend in optical communications



Silicon-on-Insulator AWG spectrometer

P. Cheben et al.
SPIE Photonics Asia,
Proceedings of the SPIE, vol. 5644,
paper 5644-17, (2004)

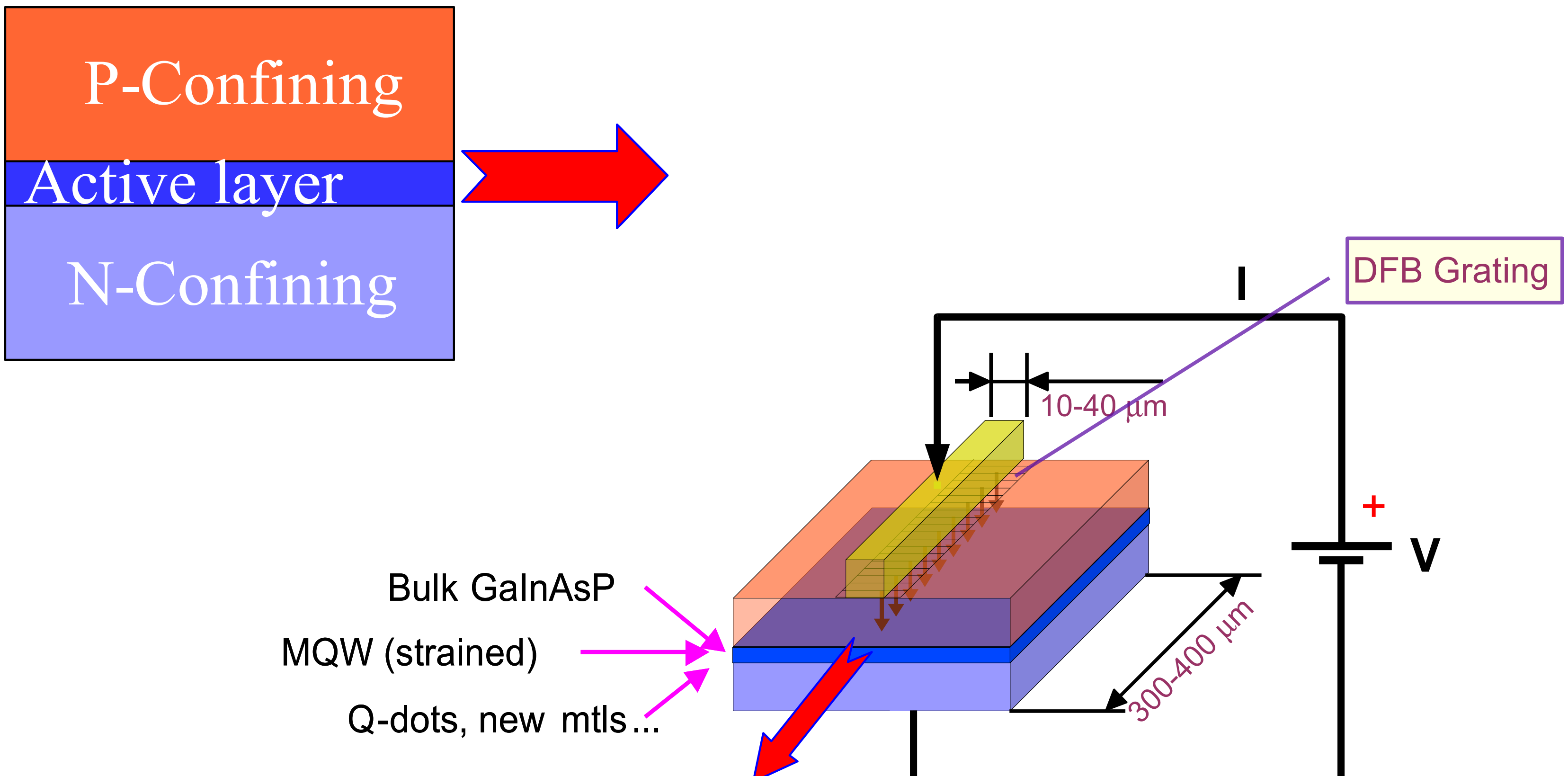
1 cm



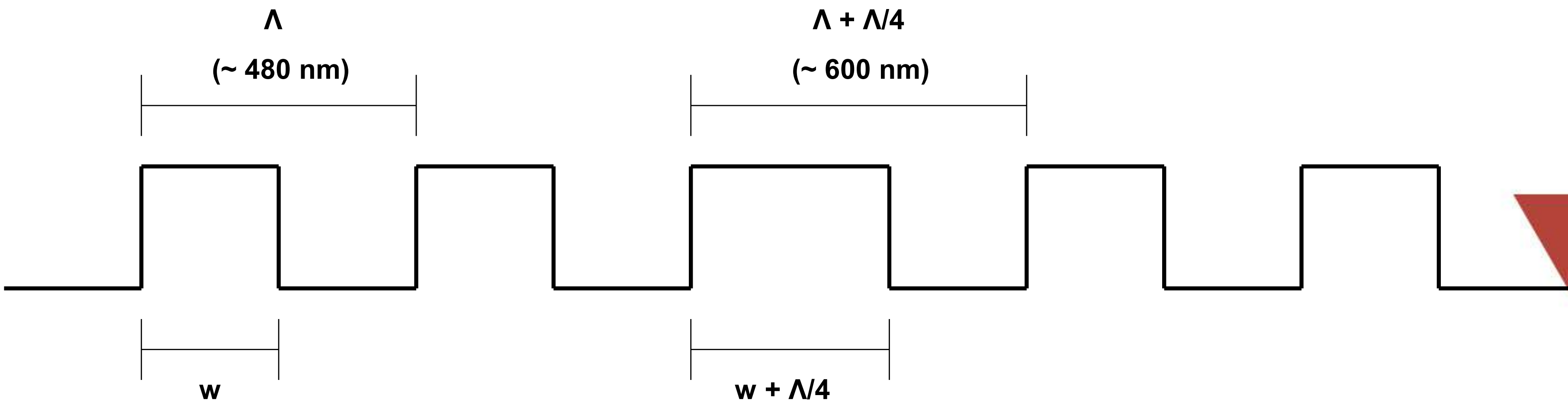
Resolution: 0.8 Å
FSR: 10 nm
Order: 80

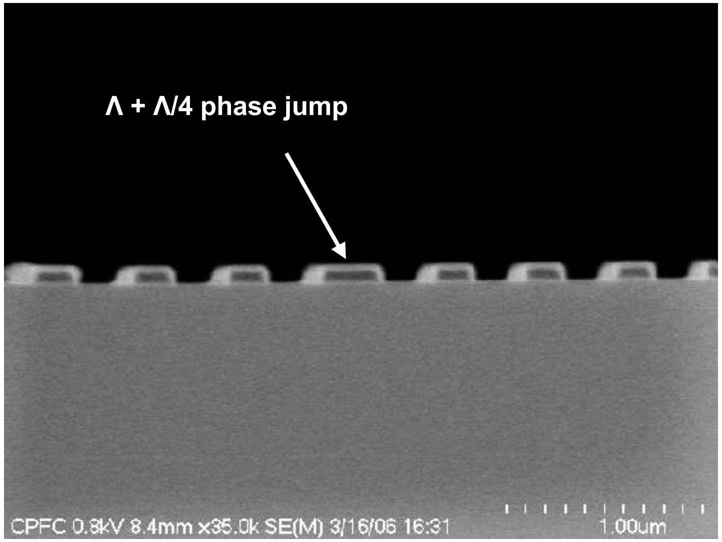
Aperture/slit defined by 0.3 µm wide trench
Waveguide separation: <1.0 µm
Channel number: 50, 2 Å

Basic DFB semiconductor laser structure

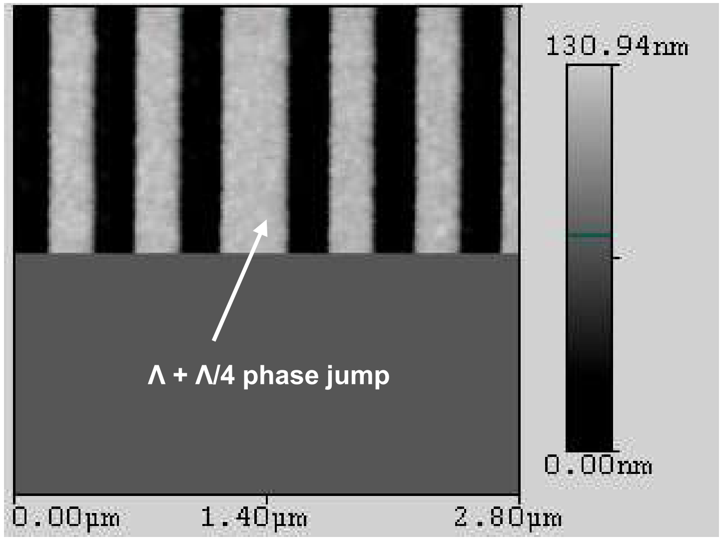


Gratings exposed in PMMA by electron-beam lithography



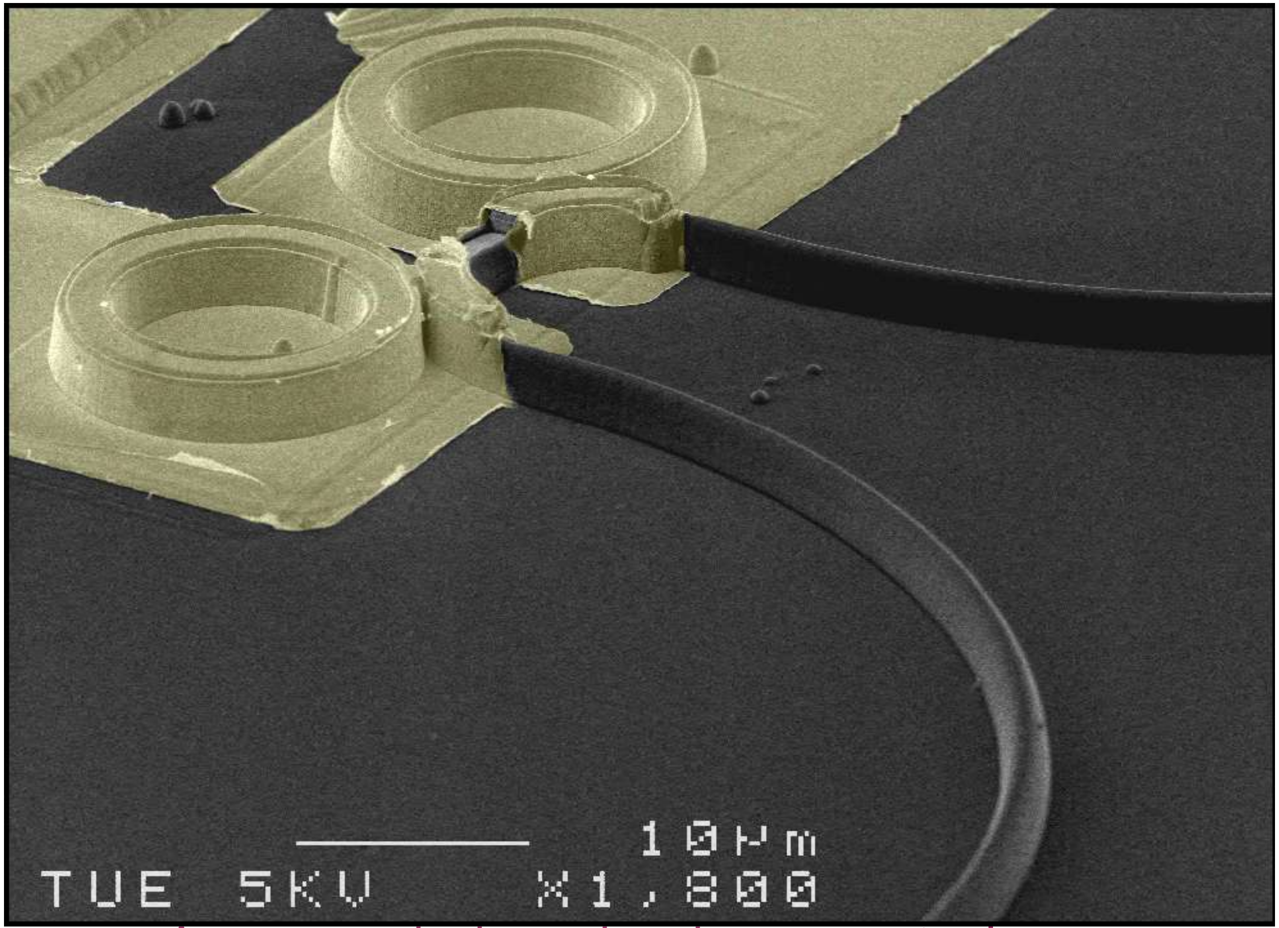


SEM cross-section of gratings in PMMA



AFM surface scan of gratings in PMMA

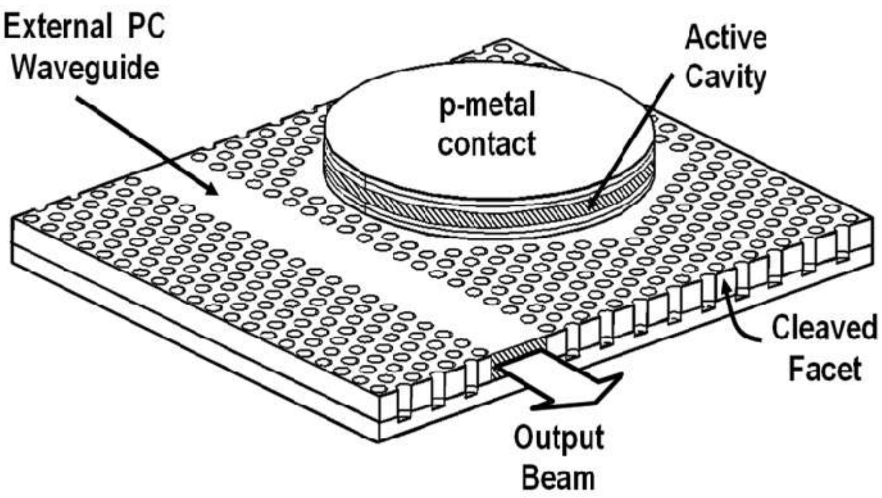
Optical memory



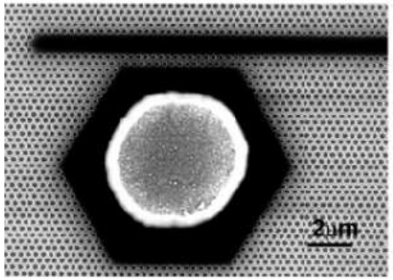
A memory device using ring resonator lasers

M. T. Hill, H. J. Dorren, T. de Vries, X. J. Leijtens, J. H. den Besten, B. Smalbrugge, Y.-S. Oei, H. Binsma, G.-D. Khoe, and M. K. Smit, “A fast low-power optical memory based on coupled micro-ring lasers,” *Nature* **432**, pp. 206–209, Nov. 2004.

Application of photonic crystals

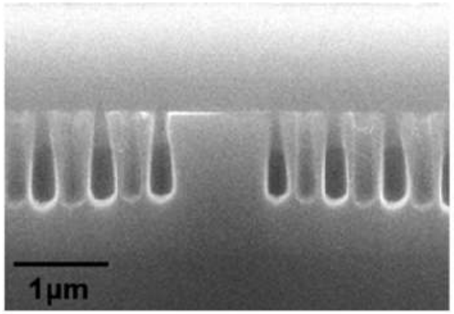


Schematic of the PC waveguide-coupled LED, where the QD active region is vertically separated from the lower guiding layer and only retained in the PC cavity region.

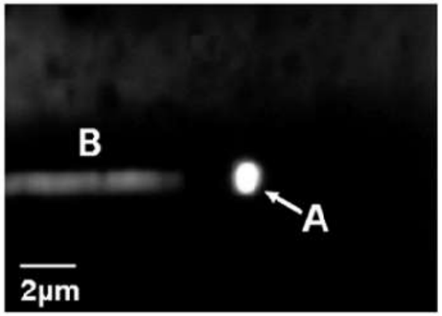


(a)

(a) SEM of fabricated device showing a top view of a complete PC cavity transversely coupled to a defect waveguide. (b) SEM of the cross-sectional view of the air holes of the 2-D photonic crystal (left). The PC was fabricated with the lattice constant a = 340 nm, air-hole diameter d = 220 nm, and etch depth of 850 nm. (c) Near-field image of transmitted light collected at the facet of the PC waveguide, where A represents light confined in the guide and B shows the lateral leakage of light due to insufficient etch depth of air holes. The intensity of B is much weaker than that of A.



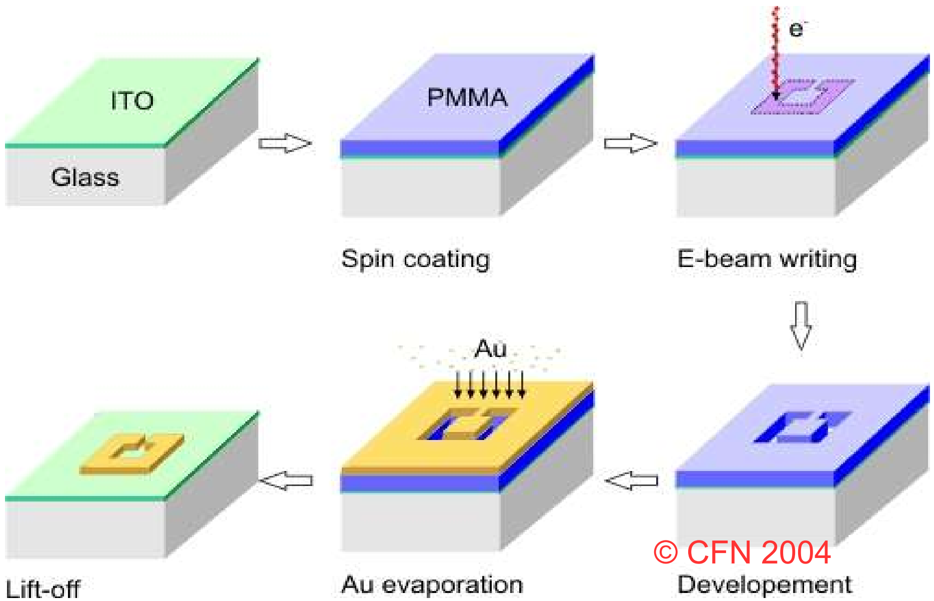
(b)

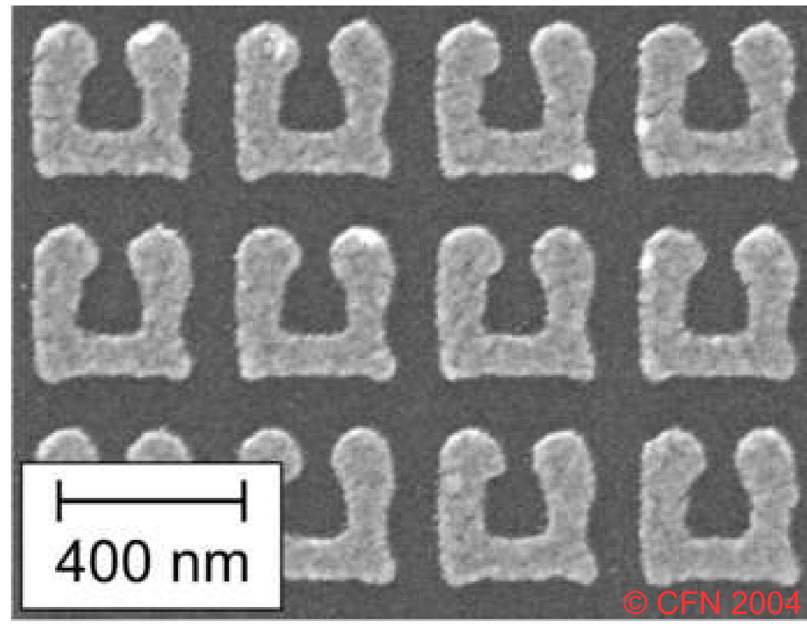


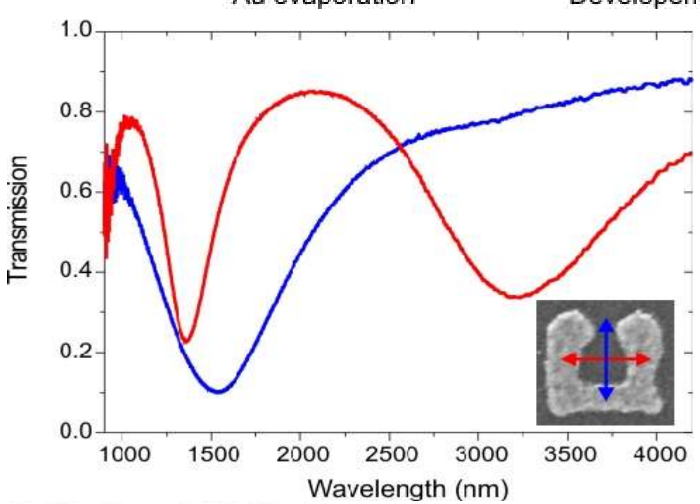
(c)

Peichen Yu, Juraj Topol´an˘cik, Swapnajit Chakravarty, and Pallab Bhattacharya, *Mode-Coupling Characteristics and Efficiency of Quantum-Dot Electrically Injected Photonic Crystal Waveguide-Coupled Light-Emitting Diodes,* IEEE JOURNAL OF QUANTUM ELECTRONICS, VOL. 41, NO. 3, MARCH 2005, p.455

Photonic Crystal Metamaterials







Transmission spectra of an array of SRR for two orthogonal linear polarizations. The arrows in the inset indicate the directions of the incident electric field vectors for the two spectra.

S. Linden, C. Enkrich, M. Wegener, J. Zhou, T. Koschny, and C.M. Soukoulis, Magnetic Response of Metamaterials at 100 Terahertz, Science 306, 1351 (2004)

Challenges in nanophotonics fabrication

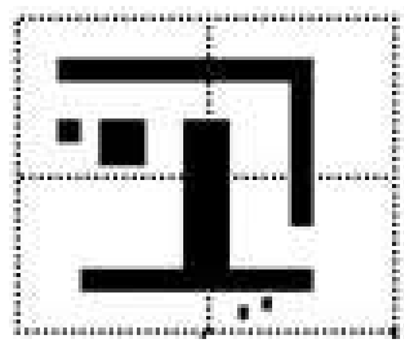
- Feature size down to 0.05 μm
  - **Photolithography** becomes non-practicable due to the HIGH co$t of ownership
  - **E-beam lithography** – for small-scale and pilot production
  - **Nanoimprint** – a solution for mass production in nanophotonics
- Devices may be few centimetres large
  - Needs multi-field exposure both for EBL direct write and for imprint template writing – field stitching errors should be minimized to avoid light scattering and reflections.
  - Requires high placement accuracy to maintain device optical coherence over large distance
- Strict edge roughness requirements to minimize losses in the waveguides
  - Resist mask edge roughness control
    - Shot noise optimization
    - E-beam position jitter minimization
  - Smooth etch techniques for waveguide etching

Metrology in nanophotonics fabrication

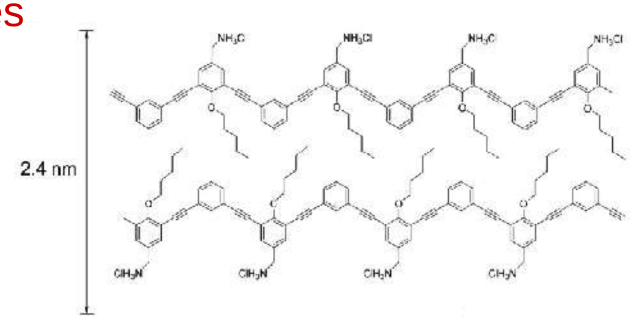
Parameter	Measurement method	Accuracy factors	Reference
Feature size, lateral critical dimensions	SEM, AFM	**SEM:** scale calibration; specimen charging; scanning field distortions; electronic jitter, acoustic and EM interference. **AFM:** XY-scale; scanner linearity; scanner orthogonality; tip shape influence and degradation; acoustic interference.	**SEM:** lithographically made or self-assembled conductive reference objects. **AFM**: objects with known 3D topography for tip shape assessment and periodical 1-2D structure for scanner calibration
Step height and film thickness	AFM, contact profiler, optical profiler, optical interferometer, ellipsometer	Scale calibration; vibrations; accurate refraction index data	Thickness gauges; laser light wavelength
Grating pitch (local)	SEM, AFM	Same as above	Same as above
Grating pitch (averaged)	Diffraction, Littrow angle measurement	Laser light spacial coherence and spectral width. Angular measurement accuracy	Reference diffraction gratings
Grating duty cycle (local)	SEM, AFM	Same as above	Same as above
Grating duty cycle (averaged)	Reflectometry	Film thickness uniformity	Relative measurement
Edge roughness	SEM, AFM	Tools resolution, availability of the image processing software	Self-assembled structures can be used as a roughness reference

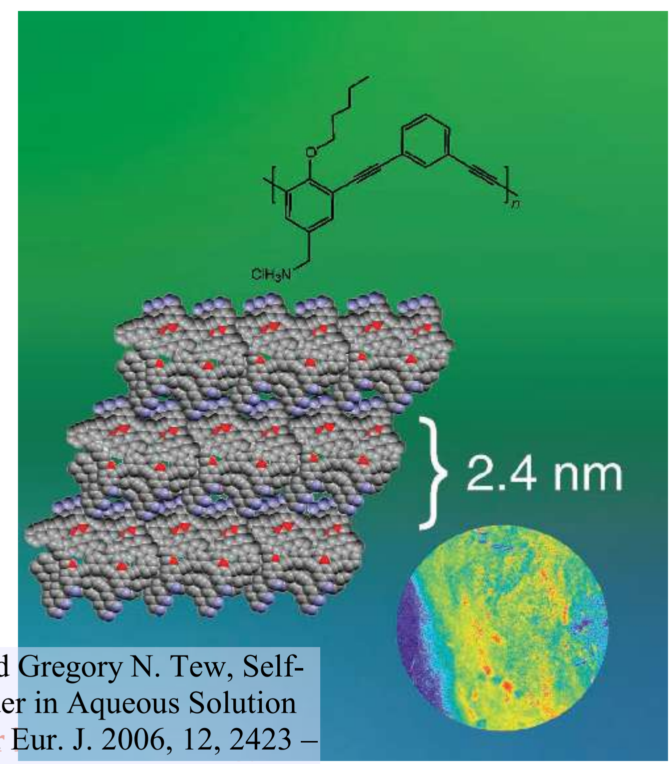
Nanometre reference fabrication methods

- Microlithography
  - Photolithography
  - Electron beam lithography
  - Nanoimprint
  - Holography



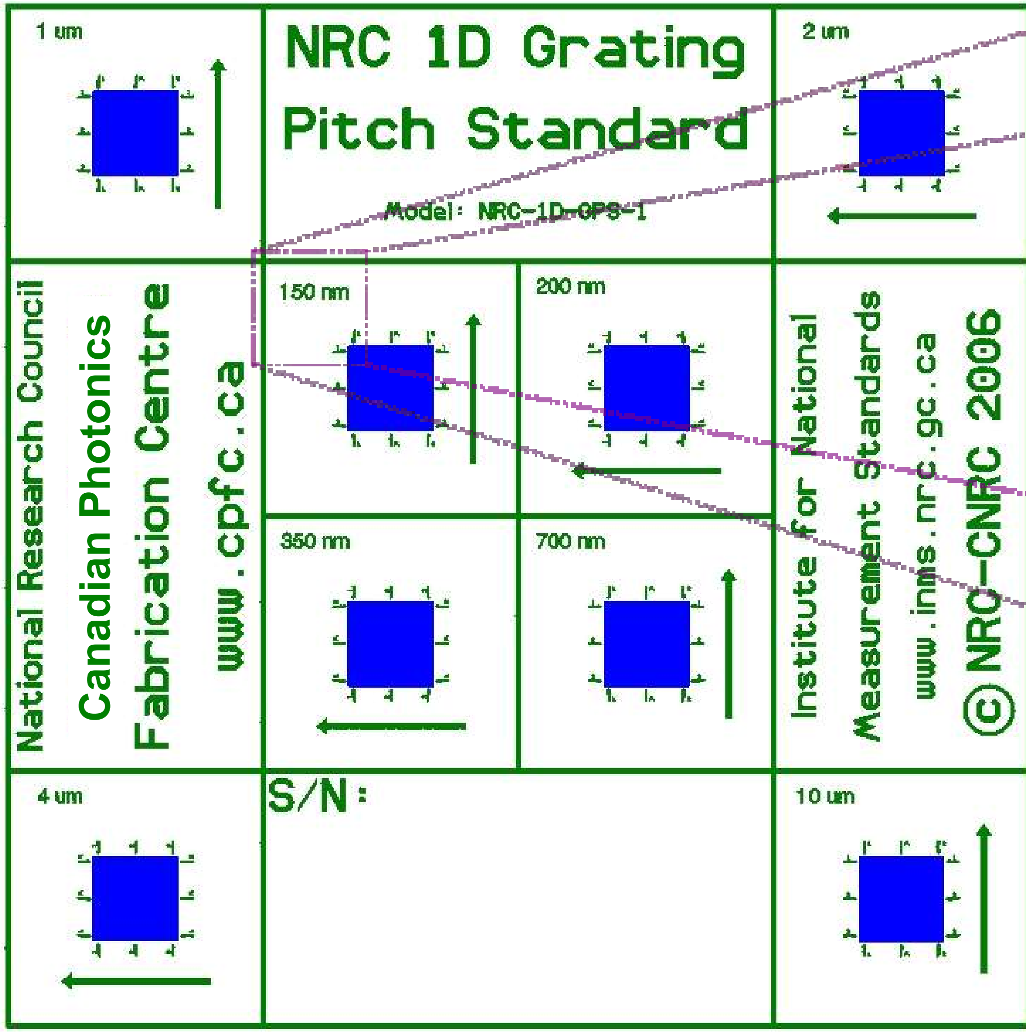
- Self-assembled structures
  - Organic molecules
  - Biomolecules, etc.
  - Nanoparticles
  - CNTs



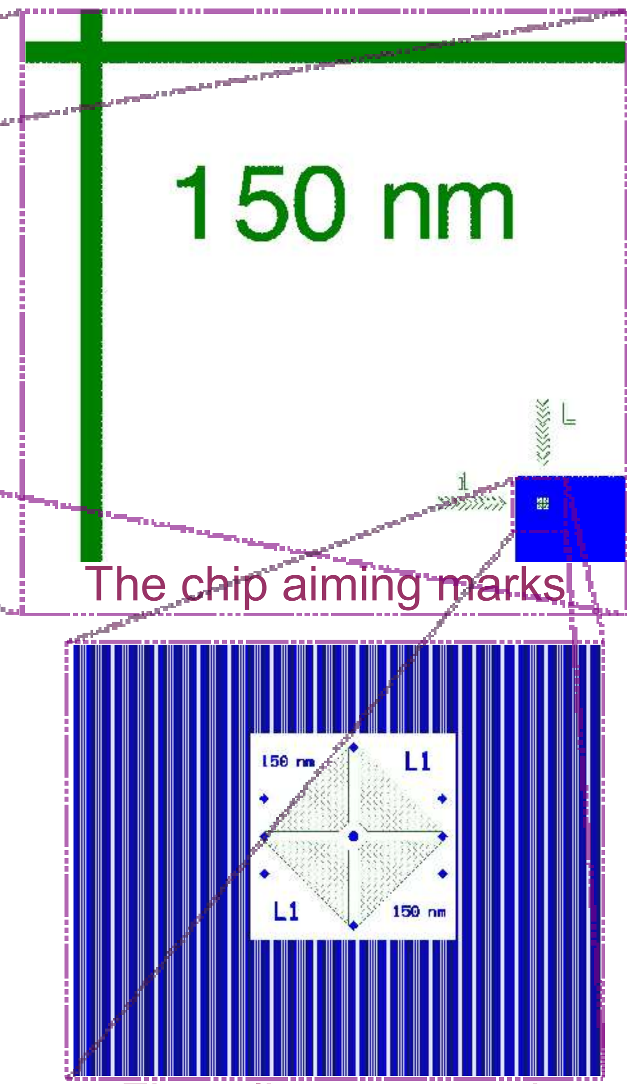


Taehyung Kim, Lachelle Arnt, Edward Atkins, and Gregory N. Tew, Self-Assembled Structures with Liquid-Crystalline Order in Aqueous Solution by Patterning Poly(phenylene ethynylene)s, Chem. Eur. J. 2006, 12, 2423 – 2427

Nanometre reference chip fabrication at NRC



Reference chip design developed by INMS/NRC



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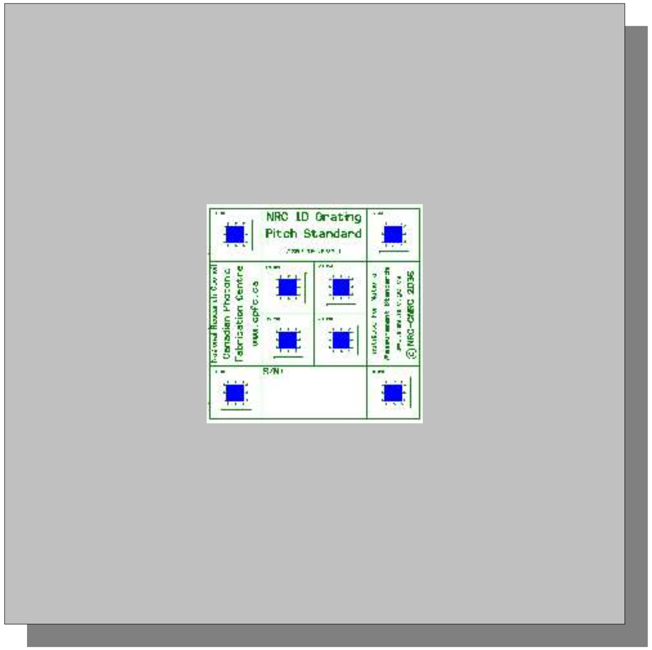
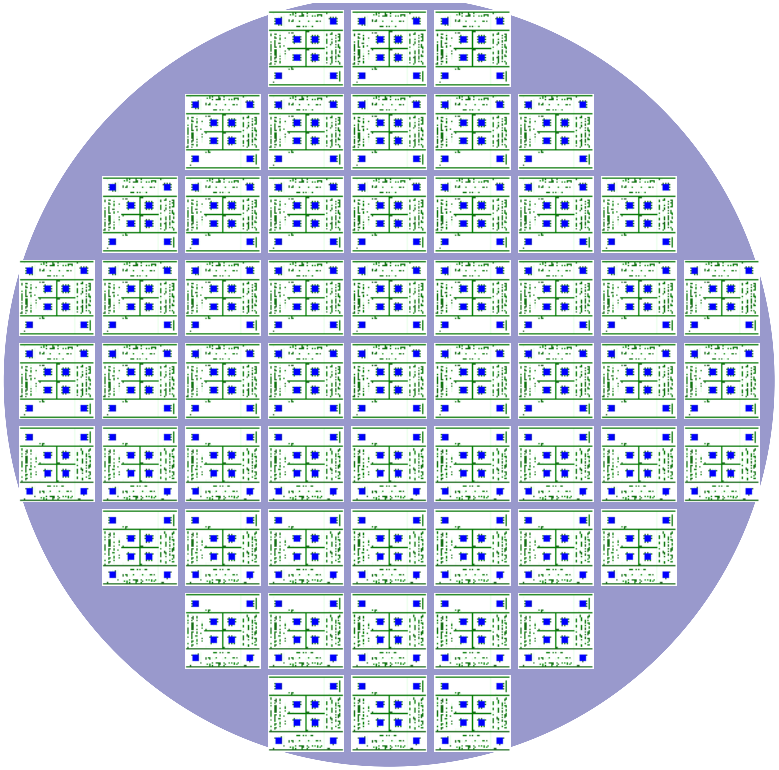
Fabrication of reference chips at CPFC

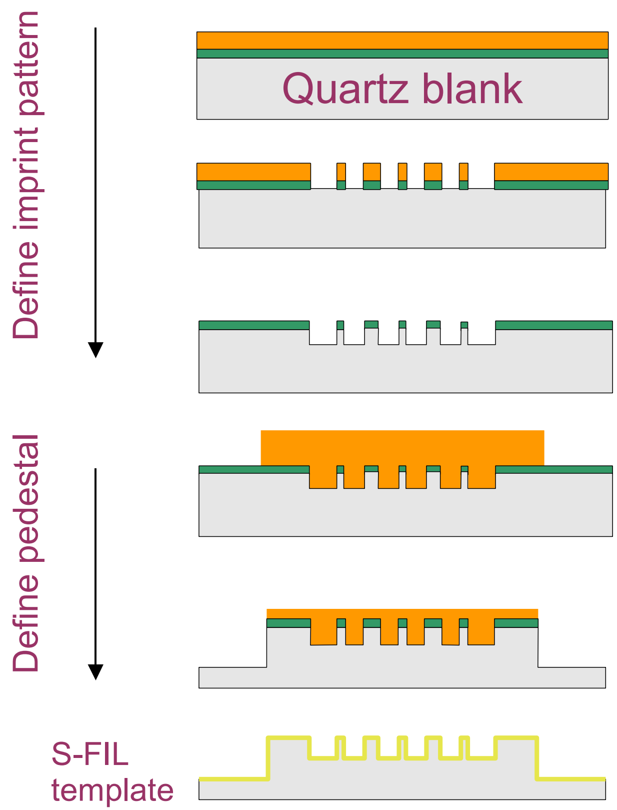


A template for S-FIL is fabricated



The template is used to imprint the chip in 55 locations on a 4" wafer

S-FIL template fabrication



A quarz blank is sputter coated with a 10-20 nm thick film of metal and then e-beam resist is spun on.

E-beam exposure is performed, resist developed, and the metal film is etched in a RIE process.

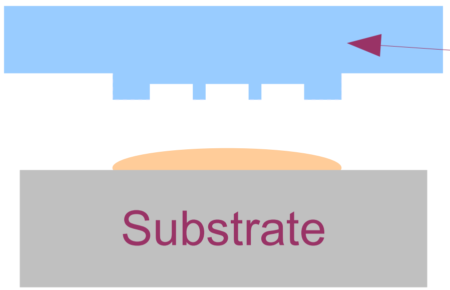
Second RIE is used to etch quartz blank to a specified depth with a specified slope angle.

A thick layer of photoresist is spun on the blank and photolithography exposure is done to define the pedestal.

Pedestal is wet etched to the depth of 15 $^{+- 0.1}$µm

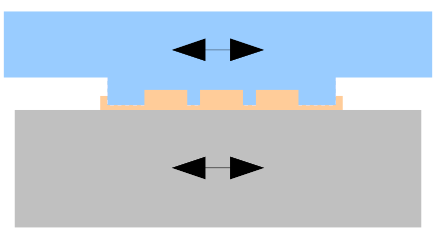
Photoresist and metal are chemically removed and the template is coated with antisticking monomolecular layer

Step and Flash Imprint Lithography

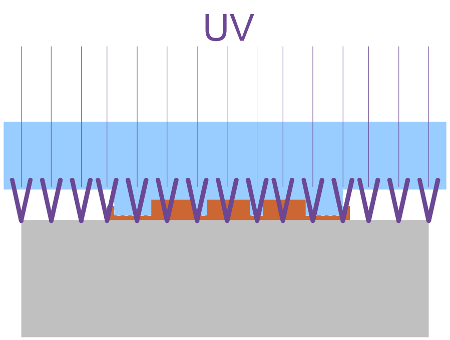


Quartz template with pedestal, made with EBL

A drop of a liquid monomer with the approximate size of the pedestal is placed onto the substrate.

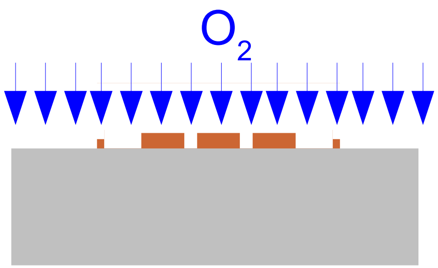


The template and the substrate are brought into contact and aligned with high precision using an optical microscope.

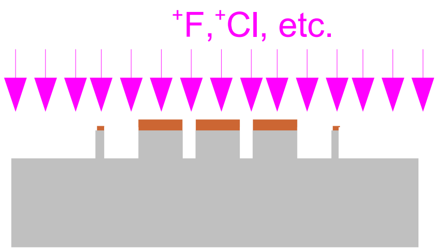


After the alignment is done the monomer is flood exposed with UV light through the template and as a result gets polymerized.

Template is released and a polymer mask remains on the substrate

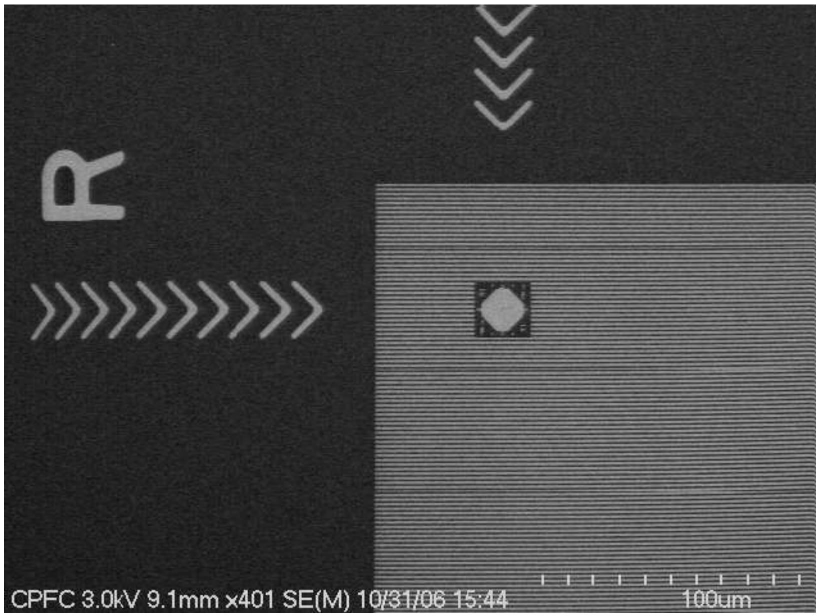


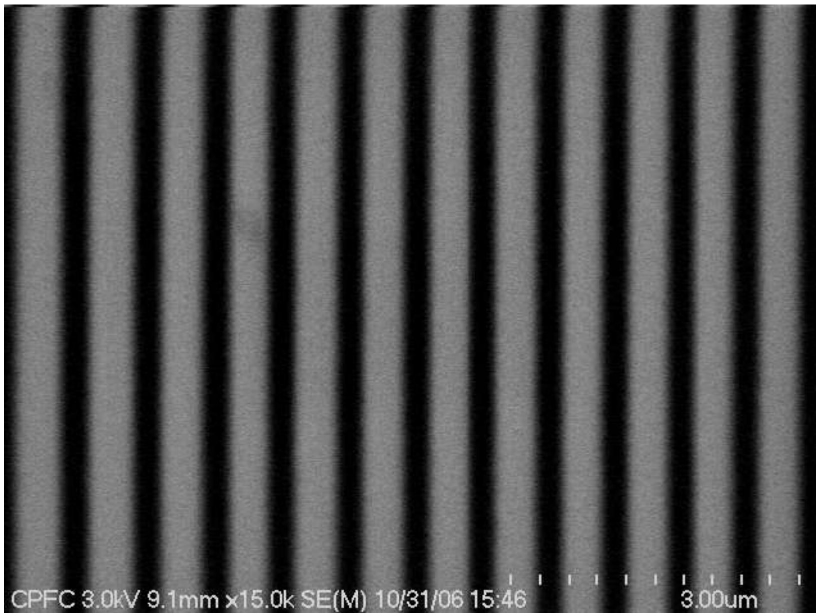
A thin residual layer is removed by a RIE process



Obtained polymer mask can be used, e.g., for a subsequent substrate plasma etching or any other image transfer procedure.

First results for grating pitch standard fabrication



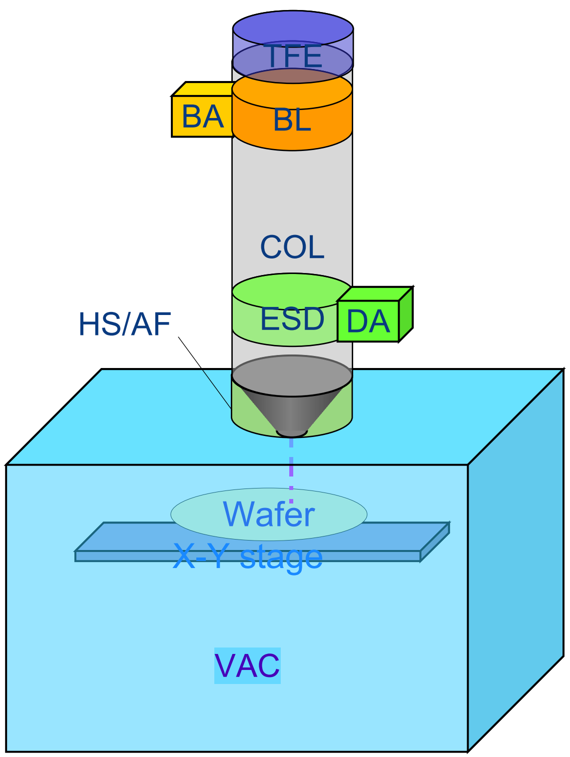


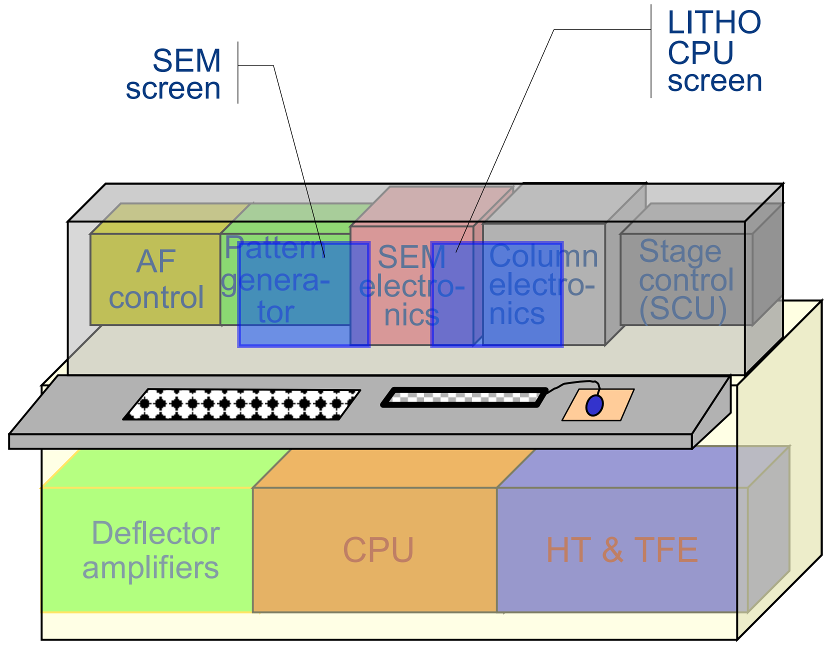
Aiming mark and a fragment of 700 nm pitch grating etched in 30 nm thick layer of chrome

Closing comments

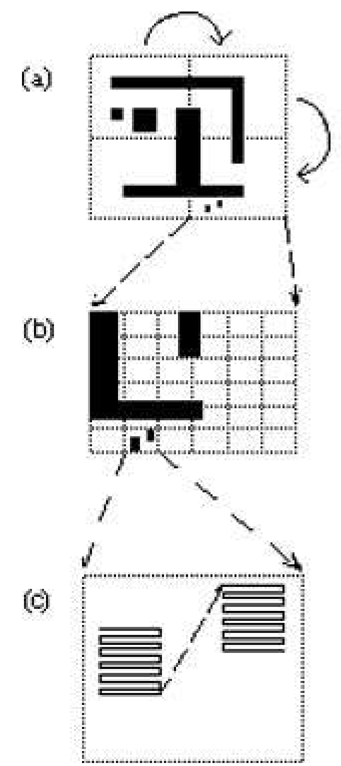
- Modern photonic devices follow electronic ICs in their trend of miniaturization towards nanometre dimensions
- Methods of nanophotonic devices fabrication include techniques uncommon (so far) to the main stream semiconductor industry, such as direct write electron beam and nanoimprint lithographies.
- Metrology in photonic fabrication is critical on both large (cm) and nanometre scales and involves variety of measurement methods
- Methods of nanofabrication have to be used for metrology reference specimens manufacturing
- NRC (INMS & CPFC/IMS) has started along the route with manufacturing of the grating pitch standard by electron beam lithography and nanoimprint

Electron beam lithography





* Laser interferometer stage
  Accuracy – λ/1024 = 6.5 Å
* E-beam position feedback with actual stage position
  Feedback update rate ~ 1M/s
* Stage is a reference for deflector gain and rotation calibration
* Maximum field size 800 x 800 mm²
* Minimum beam diameter 4 nm @ 50 kV
* Resolution in resist 30 nm half pitch



The vector-scan writing strategy.
a) Chip level
b) Field level
c) Subfield level or primitive